KEITHLEY

Model 4200-PIV Measurements

Application Note

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Model 4200 Pulse IV Measurements for CMOS Transistors

What is Pulse IV?

Pulse IV provides a user with the capability of running parametric curves on devices using pulsed rather than DC signals. A pulse source with a corresponding pulse measurement can be used in two general ways.

The first method is to provide DC-like parametric tests, where the measurement happens during the flat, settled part of the pulse. Typical tests are IV sweeps, such as a Vds-Id family of curves or a Vgs-Id curve used for Vt extraction.

The second method is transient testing, where a single pulse waveform is used to investigate time-varying parameter(s). An example of this second case would be using a single pulse waveform to investigate the Id degradation versus time due to charge trapping or self-heating.

Why use Pulse IV?

Both methods of Pulse IV testing listed above are typically used to overcome or study the effects of self-heating (joule heating) and for time-domain studies, such as transient charge trapping in the device under test (DUT). As a general trend, pulse and pulse IV testing is increasingly important in semiconductor research, device and process development.

This document will focus on the DC-like IV sweep capability of the 4200-PIV package, although other types of pulse testing are possible, such as charge pumping, single pulse charge trapping, AC stress, and non-volatile memory testing.

What is the 4200-PIV Pulse IV Package?

The 4200-PIV Pulse IV package is an optional factory-installed kit for the Keithley Model 4200-SCS. The focus for the 4200-PIV package is testing lower power CMOS transistors that exhibit self-heating or charge trapping effects.

Self-heating has been an issue for some higher power devices, but is emerging as a problem for lower power devices based on smaller dimensions and silicon-on-insulator (SOI) technology, where it is more difficult for the heat generated by the transistor to leave its immediate surroundings.

In addition to smaller dimensions, high κ materials are being considered to greatly lower gate leakage current for future transistor technology. Unfortunately, these high κ materials and related integration processes are not yet perfected and have both interface and bulk lattice imperfections that can cause charges to be trapped.

Both the charge trapping and self-heating effects can be largely avoided by using pulse IV instead of DC parametric testing.

To accomplish pulse IV testing of CMOS transistors, the 4200-PIV package consists of:

• 4200-PG2	Dual channel voltage pulse generator
• 4200-SCP2	Dual channel oscilloscope
• Pulse IV Interconnect	4200-RBT Remote Bias Tees to combine both DC and pulse signals and necessary cables and connectors
• Pulse IV software	Projects and test routines for testing of CMOS transistors, including cable compensation and load-line algorithms to provide DC-like sweep results

The configuration and test concepts of the 4200-PIV package are based on concepts and work by K.A. Jenkins[1] and A. Kerber[2], with results by C.D. Young[3] and others.

Target Applications and Test Projects

The 4200-PIV package includes test projects that address the most common parametric transistor tests: Vds-id and Vgs-id. These tests are provided in both DC and Pulse modes, allowing correlation between the two test methods, and have been configured for testing leading edge, lower-power CMOS devices.

These tests, as well as initialization steps for scope auto-calibration and cable compensation, are included in a single 4200 test project, Pulse IV-Complete.

There is another Pulse IV test project, Demo-PulseIV. This Demo project is a subset of PulseIV-Complete and is intended for demonstrating the Pulse IV capabilities using a packaged demonstration DUT.

Overall 4200 Pulse IV capabilities

- Pulse voltage on gate from -5 to +5V, zero referenced
- Pulse widths of 40-150 ns (due to 4200-RBT), adjustable in 10 ns increments
- Periods of 40 us and larger (due to 4200-RBT), adjustable in 10 ns increments. The maximum duty cycle is 0.1%.
- Pulse transition is programmed to 10 ns, which results in a 13 ns transition time.
- DC voltage bias on drain, provided by SMU, from -210V to +210V.
- Drain current pulse measurement, up to 100 mA with 5 uA resolution (lower resolution available by averaging multiple pulses) provided by 8 bit scope card.
- Vds-Id and Vgs-Id sweeps
- Single pulse “scope” shot for setup validation and transient testing

Note that the above list is specific to the operation of the entire 4200-PIV package. The individual components, such as the 4200-PG2 and 4200-SCP2, may have different capabilities. For example, the 4200-PG2 can be programmed to output a 10 ns wide pulse, but this pulse is not sufficient for a Pulse-IV measurement and is therefore not permitted in the supplied PIV setup.

Theory of Operation

This document complements the information in the Pulse IV portion of section 4 in the 4200-SCS Applications manual. All 4200 documentation is available by double-clicking on the Complete Reference icon on the 4200 desktop.

In general, the 4200-PIV applies a pulse to the gate, while DC biasing the drain. The source and body connections are connected to ground/shield. The dual channel oscilloscope (4200-SCP2) measures the gate voltage and drain voltage. The drain current is calculated by the voltage drop across the 50 ohm termination of the scope (Figure 1a, Rsense on SCP2 Channel 2).

Figure 1a and 1b show a schematic diagram of the Pulse-IV setup with corresponding waveforms from select points in order to provide snapshots of the signals and to show the effects of various aspects of the setup. Although many waveforms are displayed below, there are only 2 waveforms that are actually measured by the 4200-SCP2 (B and E). The waveforms shown in Figure 1b are a snapshot of the signals shown in Figure 1a, all graphed on the same time scale. Showing all waveforms together permits comparison of the DC offset and relative amplitudes in various parts of the schematic.

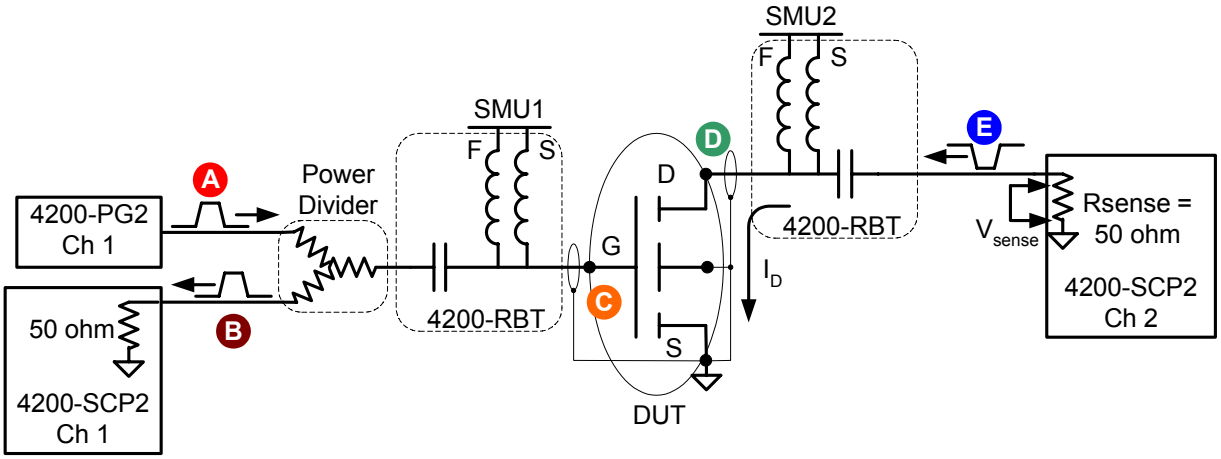

Figure 1a. 4200 Pulse IV interconnect schematic, showing 4200-PG2, 4200-SMUs, 4200-RBTs and DUT.

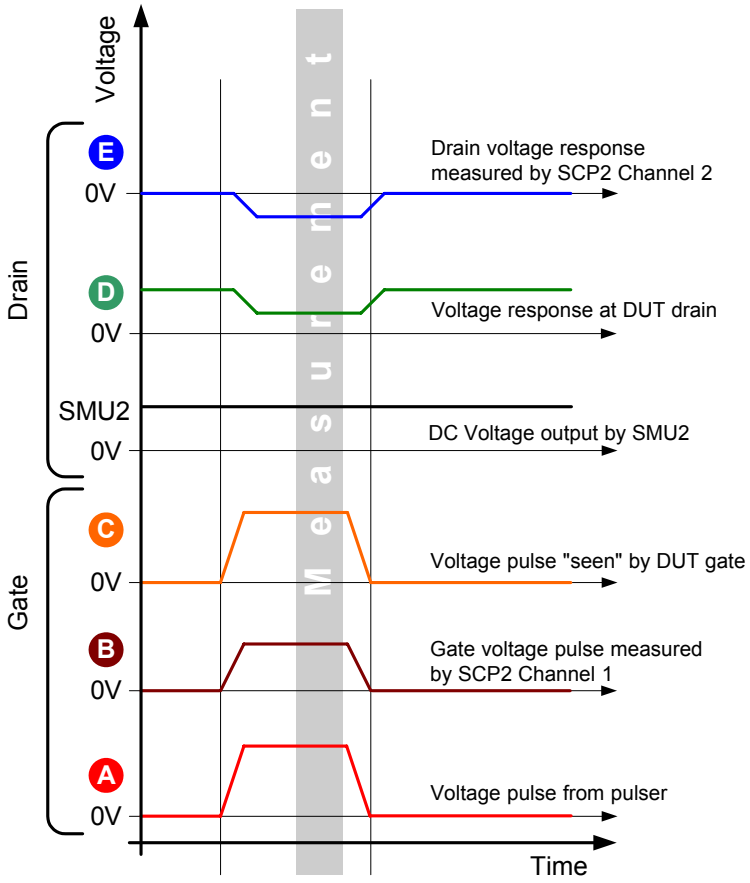

Figure 1b. Waveforms at select points in Figure 1a.

At the start of the test, the drain of the device under test (DUT) is biased with SMU2 and is waiting for a gate pulse to turn on the transistor and cause drain current, Id, to flow.

A Gate Voltage Pulse: This waveform is the output from Channel 1 of the 4200-PG2. Its amplitude is about the same as that seen by the DUT gate (C), except for some small cable losses. Note that there is no DC offset on this waveform, as any DC voltage would cause excessive power to be dissipated in the power divider.

B Gate Voltage Pulse measured by oscilloscope (4200-SCP2 channel 1): The portion of the pulse that is transmitted through the power divider. Because of the divider and the 50 Ω input impedance of the SCP2, the amplitude of the pulse is reduced 33%, plus any additional cable losses. The PulseIV calibration accounts for this loss caused by the power divider and cabling. The power splitter splits the power in half (3 dB), which means that the voltage is lower by the square root of 2. So asking for a 2V pulse will give a ≈1.41V signal (assuming no other losses). Note that this measurement is used to determine the proper magnitude of the V_G pulse, but it does not measure the gate current.

SMU1 (not shown in Figure 1b): This is the voltage output by SMU1 during Pulse IV testing. During pulse IV testing in the PulseIV-Complete project, SMU1 is fixed at 0V.

C Voltage pulse at DUT gate: This waveform shows what the DUT gate "sees." This is the pulse that turns on the transistor and causes the drain current to flow. The Pulse IV calibration takes into account the losses in the cabling, with the assumption that the gate is high impedance.

SMU2: DC Voltage bias applied to the drain, through the remote bias tee.

D Drain response: This waveform shows the DC bias and the resulting *response* to the gate pulse. Note that the drain is DC biased and the pulse in this waveform is the result of the gate pulse. There is no pulse applied to the drain, rather the pulse shown is the response of the drain current flowing.

E Drain voltage response measured by oscilloscope (4200-SCP2 Channel 2): The response of the drain is due to the gate pulse turning on the transistor and allowing drain current to flow. This drain current, I_D, flows through the 50 Ω input impedance of the scope, which acts as a current sense resistor (R_{sense}), resulting in the voltage drop in the waveform (V_{sense} on Figure 1a). This voltage response is negative due to the direction of current flow through the 50 Ω resistor and the fact that the scope is ground-referenced. Note that this waveform is AC shifted to 0V, due to the coupling capacitor in the 4200-RBT.

System Configuration

The 4200-PIV package adds 2 cards to the higher-numbered slots in the 4200-SCS mainframe, as shown in Figure 2. In addition, the interconnection for Pulse-IV is also shown in Figure 2 and 3.

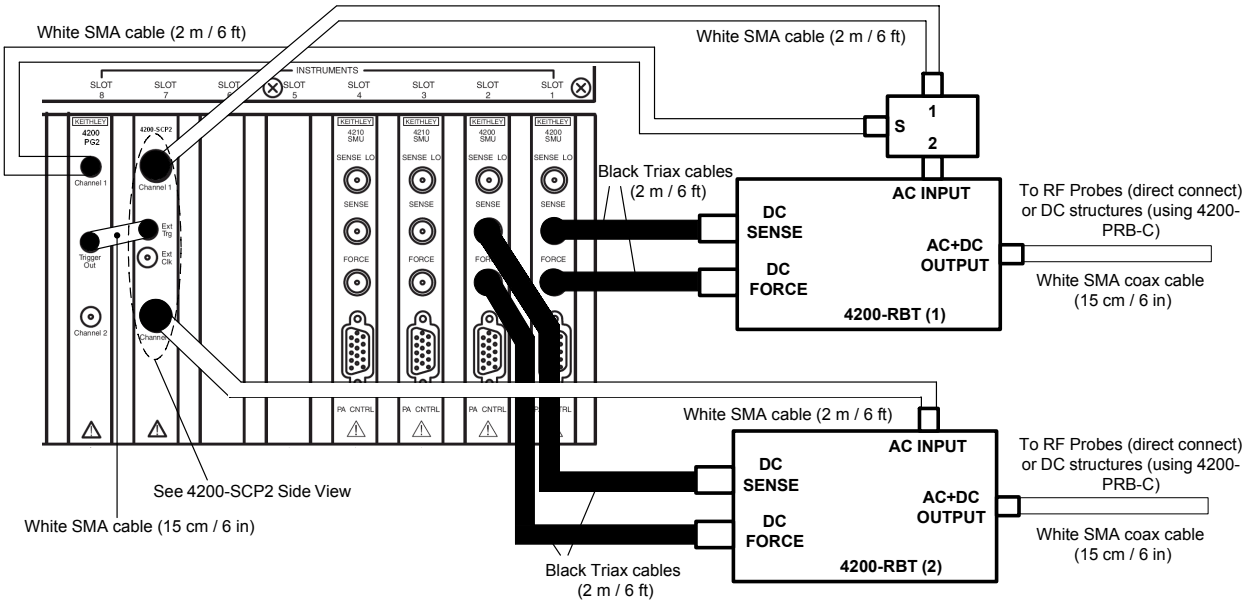

Figure 2. Connection Diagram for PIV

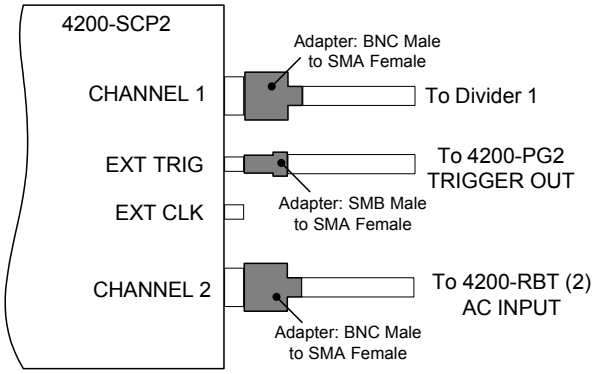

Figure 3. 4200-SCP2 Side view. Adapter details for 4200-SCP2 connections, showing adapters for BNC to SMA for the scope channel inputs and SMB to SMA for the trigger input.

4200 Project: PulseIV-Complete

This project includes all pulse source and pulse measure tests for the 4200-PIV package. This project is used for both testing on customer devices and demonstration of the 4200-PIV package.

The PulseIV-Complete project has a few Initialization steps for pulse calibration and 7 main tests under the device "4terminal-n-fet." This project permits comparison between DC and pulse IV sweeps. These 7 main tests consist of 3 pairs of tests. The first test in each pair is the DC IV sweep, with the second test using pulse IV for the sweep. The first pair is Vds-id, the second is Vgs-id and the third is another Vds-id test, but with voltages for both the gate and drain increased to demonstrate self-heating on a device. The last test, scope-shot, provides a snapshot of the pulse waveforms that are used during all pulse IV tests. Please note that the values seen in the scopeshot test are not calibrated values.

This project supports both nMOS and pMOS testing, just use the appropriate voltage sign for sourcing the proper voltage polarity.

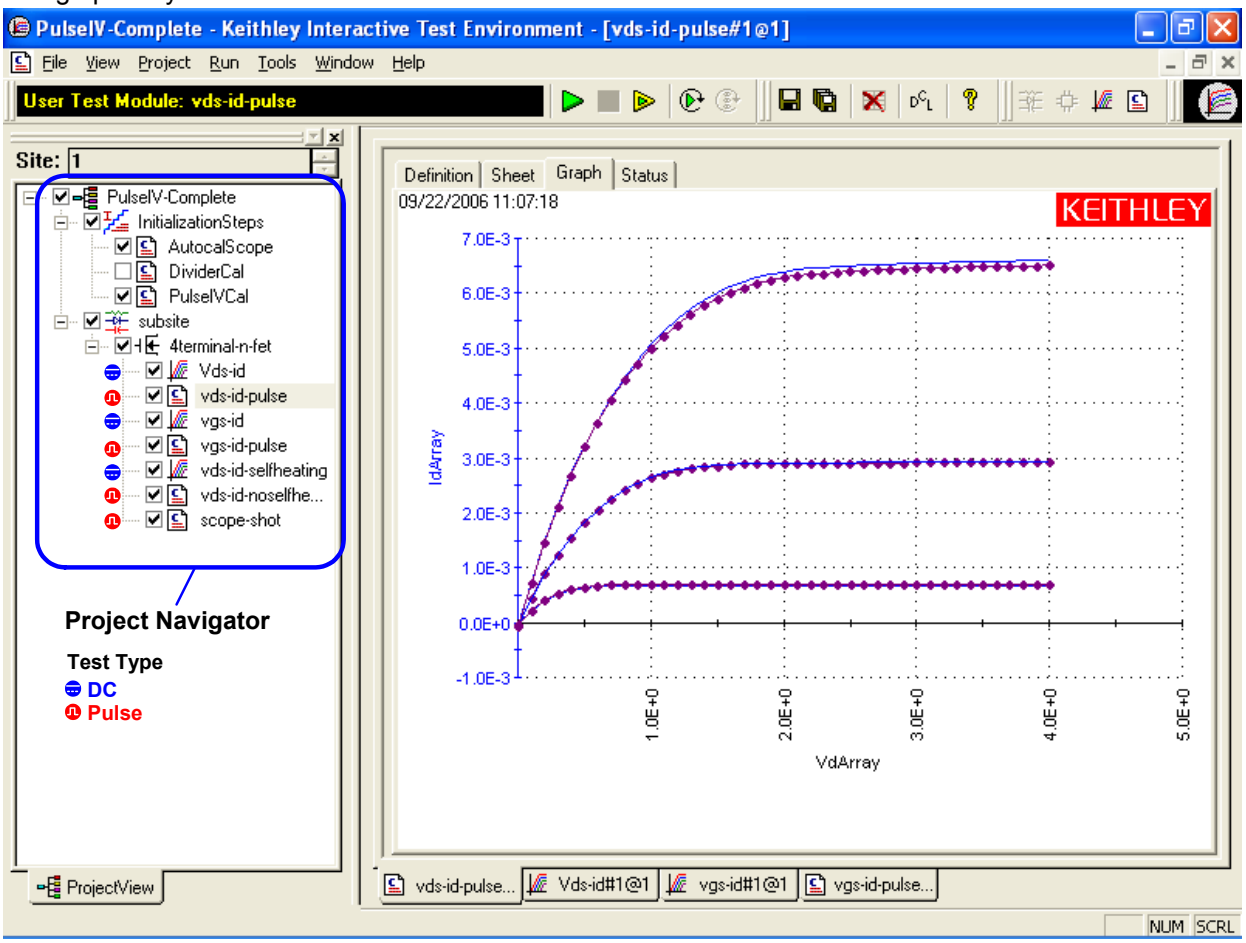

Figure 4. Screenshot of the 4200 PulseIV-Complete project, with overlay explanation for the Project Navigator.

Initialization Tests

AutocalScope – Runs the self-calibration and offset measurement routine for the 4200-SCP2. This routine should be run before every PulseIV cal and periodically to capture any drift in the SCP2. It requires all connections be removed from the scope and takes about 1 minute.

DividerCal - Use to calibrate the power divider. It is not necessary to use this cal, as the divider has already been calibrated at the factory. By default, this test is unchecked, so it is not executed during a test sequence. The DividerCal module is included here for completeness, and would only be used in the case where a divider has been replaced.

PulseIVCal - This is the Pulse-IV cable compensation routine that should be used during initial setup and whenever interconnects are changed. This routine takes about 3-4 minutes and requires changing the connection at the mid-point to transition from an open to a through (or short) connection. This routine is similar to an open/short cal used for capacitance measurements.

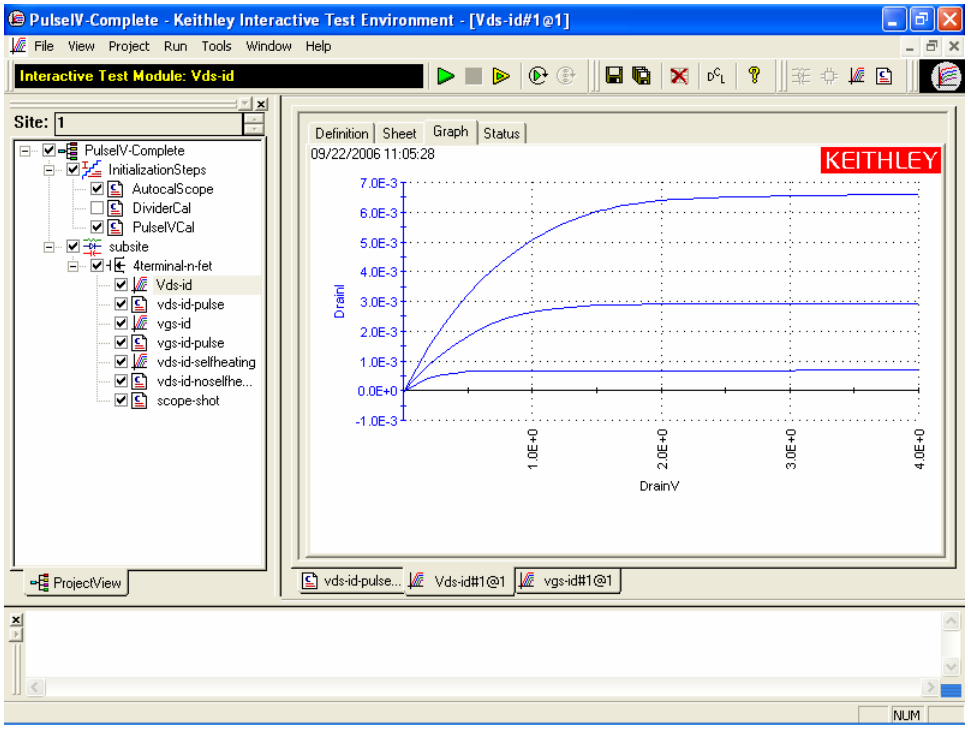

Figure 5. DC Vds-id ITM graph tab.

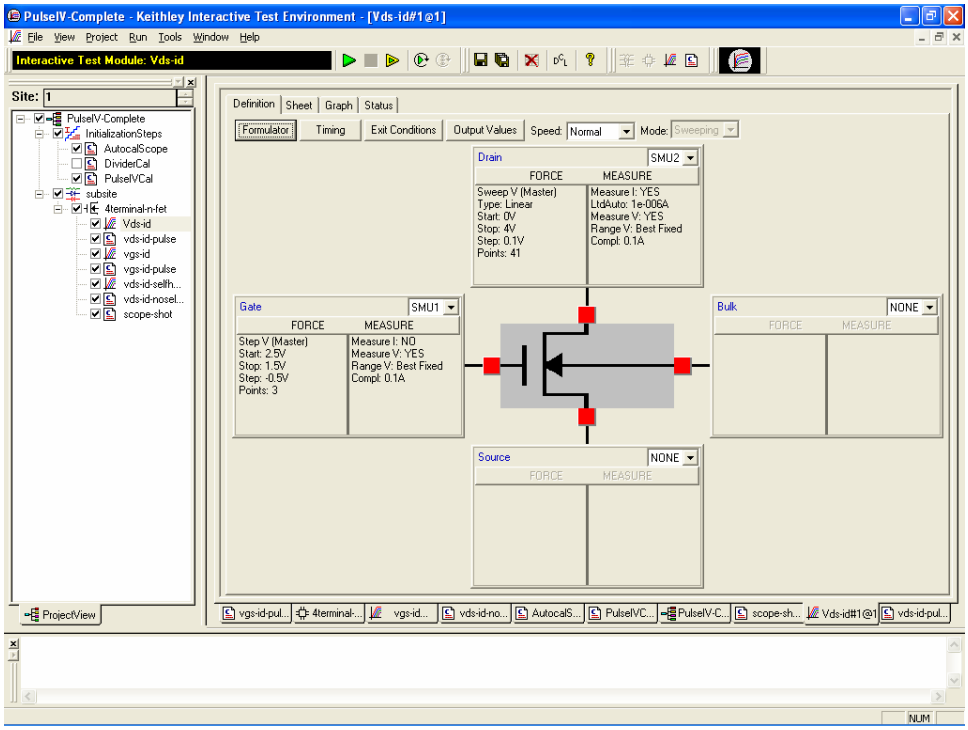

Figure 6. DC Vds-id ITM definition tab.

Vds-id

The DC Vds-id test, shown in Figure 5 and 6, is a typical family of curves. The drain voltage, V_d, is swept from 0 to 4V and after each V_d sweep the gate voltage, V_g, is stepped to the next value. The key difference between a traditional DC-only Vds-id and the DC IV through the 4200-RBT Bias Tees is the number of SMUs. For DC IV through the bias tees, 2 SMUs are used, with the Source and Body/Bulk connections connected to ground (SMA coax shield), as shown in the schematic in Figure 1a.

The Vds-id-pulse test is shown in Figure 4 and 7. Since the pulse tests are UTMs (User Test Modules), the parameters are changed via the table interface shown in Figure 7. For the pulse Vds-id, the gate voltage is not stepped, so each unique gate voltage must be entered before appending the next Vds-id curve to the graph.

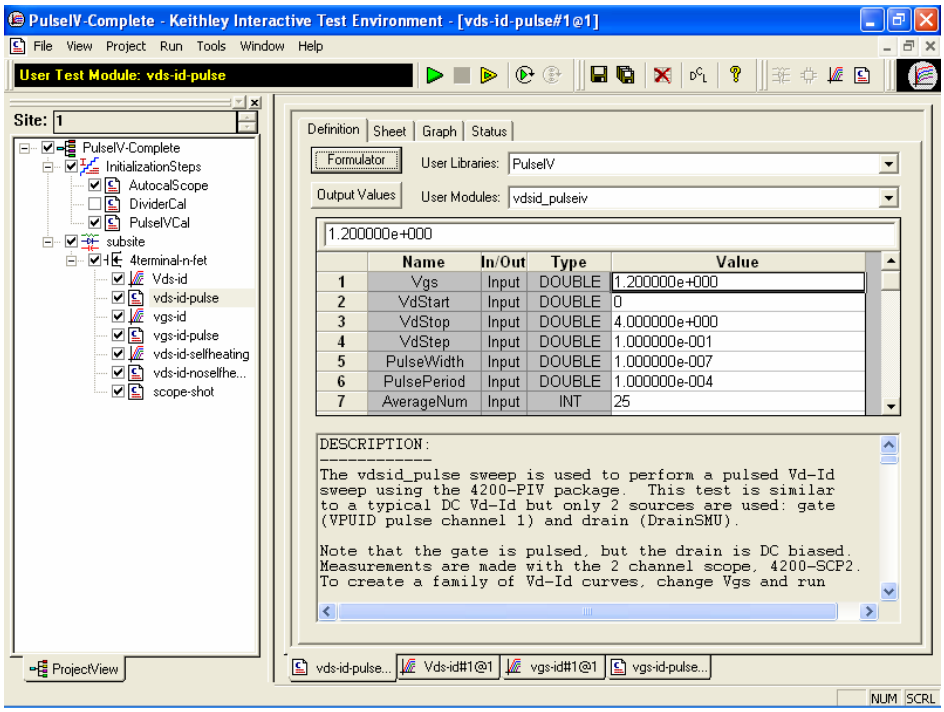

Figure 7. Pulse Vds-id UTM definition tab.

Note that both the DC and pulse test parameters are easily modified to permit interactive investigation of transistor behavior. The procedure for running a Vds-id test is covered below in Running Pulse IV Tests.

Vgs-id

The DC Vgs-id test, shown in Figure 8 and 9. The key difference between a traditional DC-only Vgs-id and the DC IV through the 4200-RBT Bias Tees is the number of SMUs. For DC IV through the bias tees, 2 SMUs are used, with the Source and Body/Bulk connections connected to ground (SMA coax shield), as shown in the schematic in Figure 1a.

The Vgs-Id-pulse test is shown in Figure 10 and 11. Since the pulse tests are UTMs (User Test Modules), the parameters are changed via the table interface shown in Figure 11.

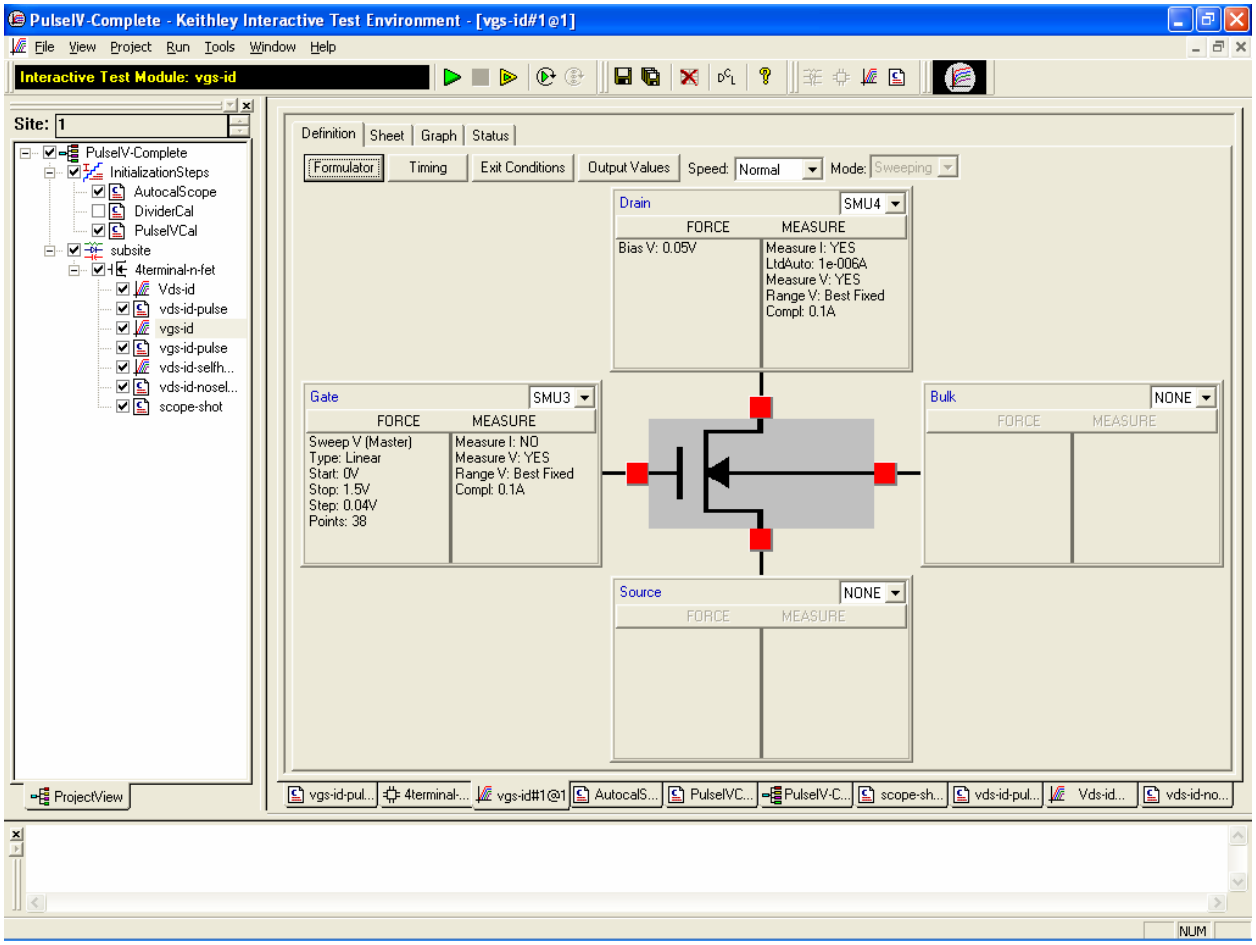

Figure 8. DC Vgs-id ITM definition tab.

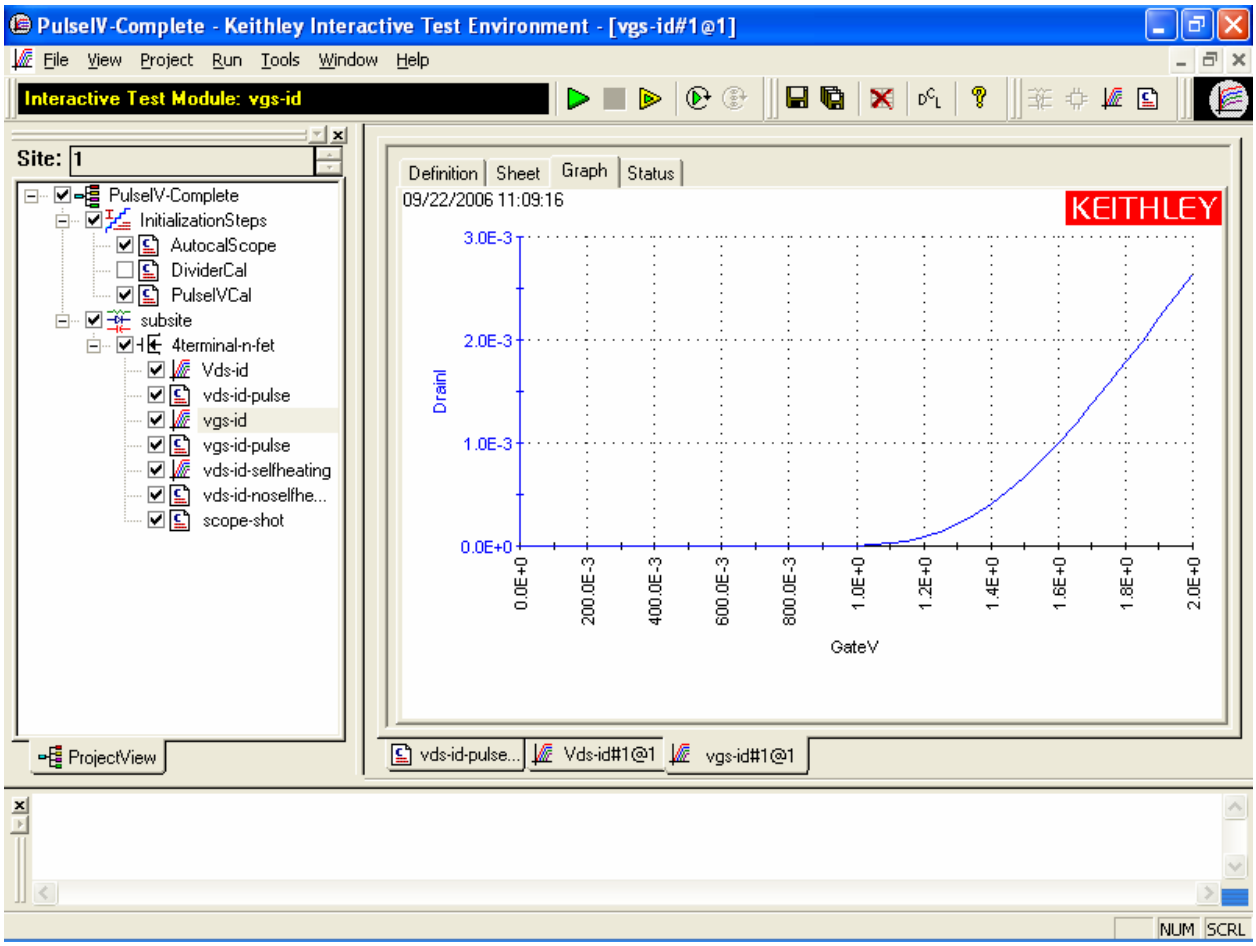

Figure 9. DC Vgs-id ITM graph tab.

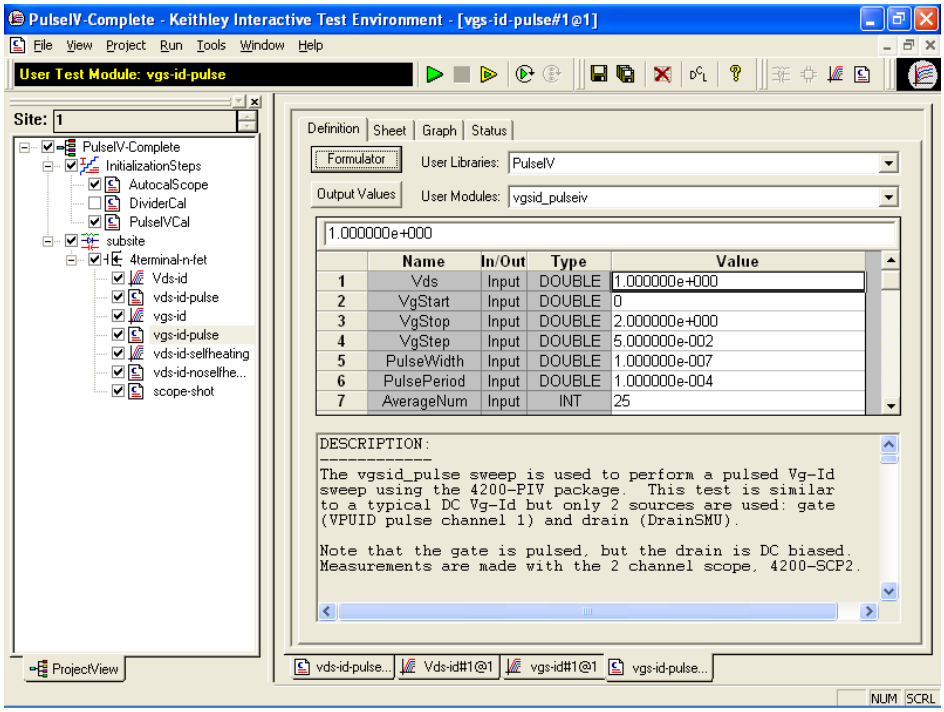

Figure 10. Vgs-id-pulse UTM definition tab.

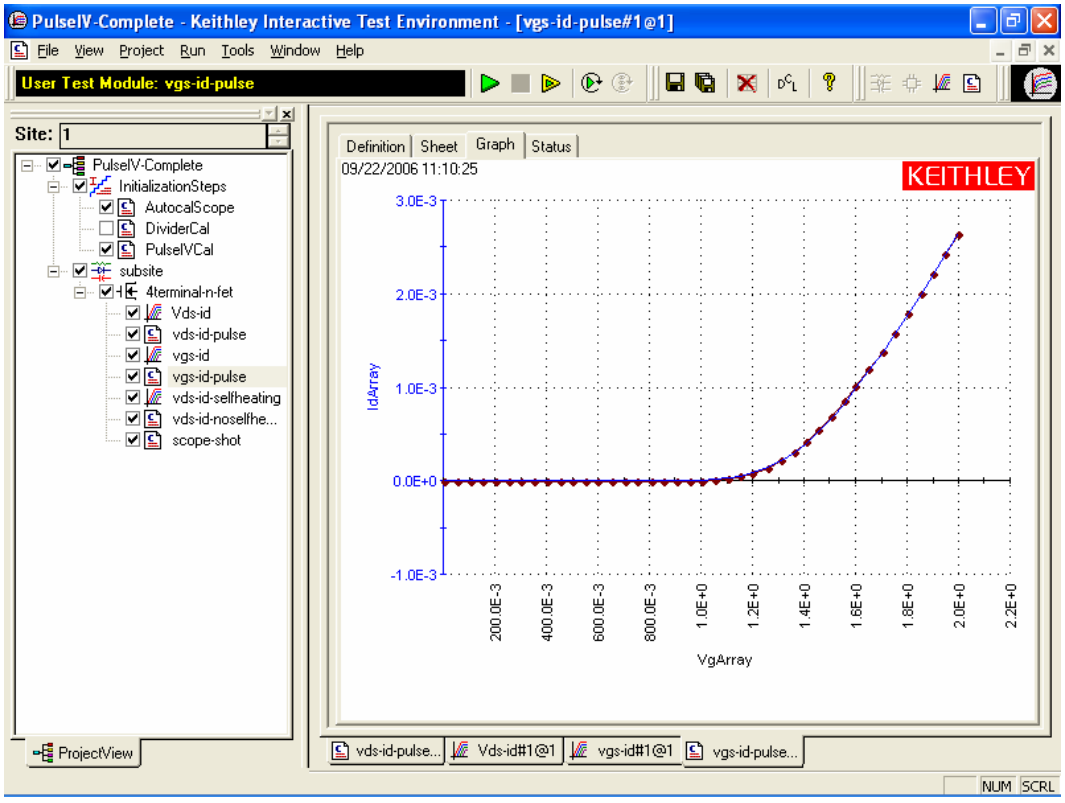

Figure 11. Vgs-id-pulse UTM graph tab.

Vds-id Self-heating and Vds-id No self-heating

This pair of projects is similar to the Vds-id DC and pulse tests described above, but with modifications to the gate and drain voltages to cause self-heating in the DC ITM test results. The pulse test uses the same parameter values, but the low duty cycle (0.1% or less) of the pulses does not heat up the DUT. Figure 12 shows the graph of the DC results with one pulse-based Vds-id curve overlaid.

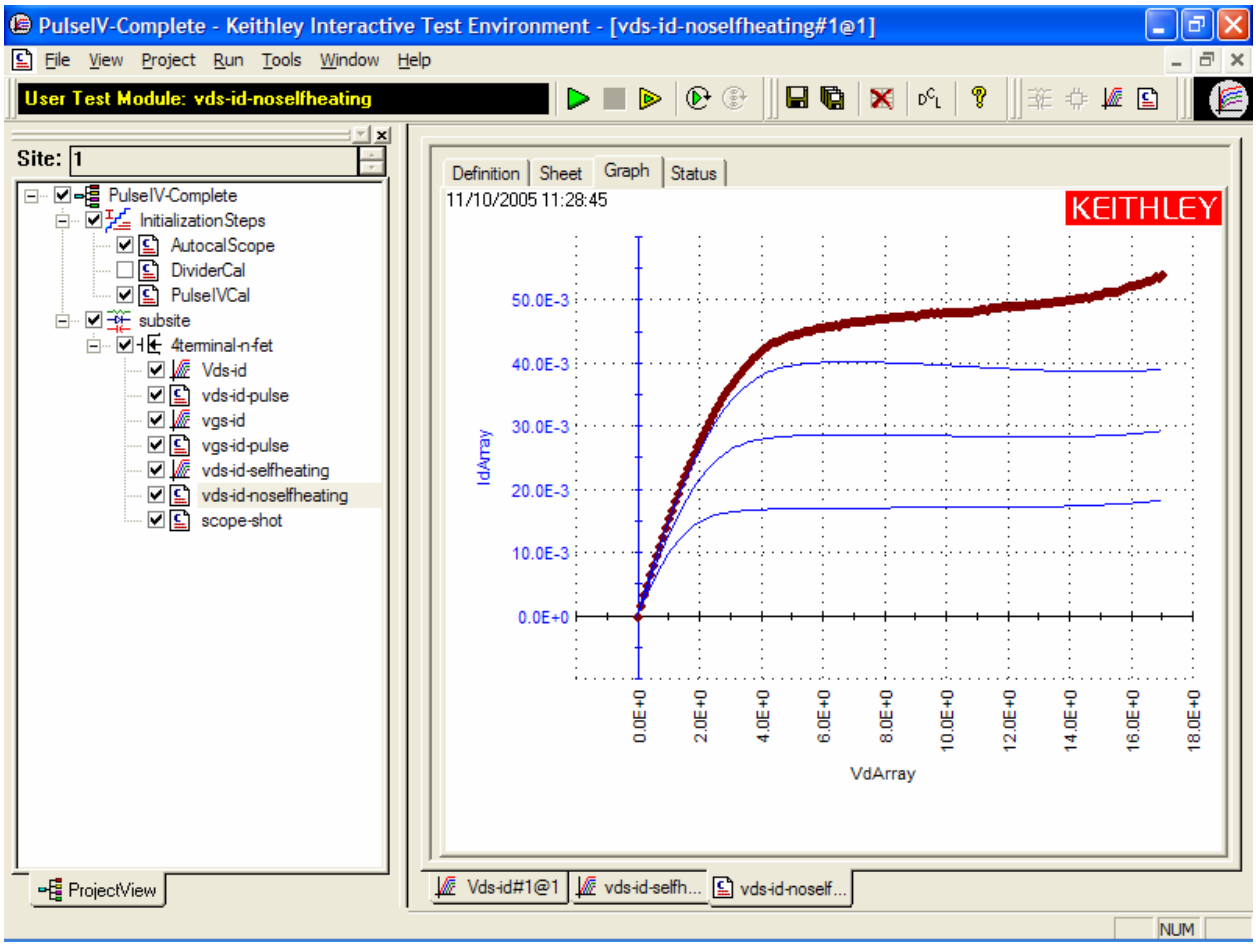

Figure 12. Vds-id-noselfheating UTM graph tab. The wider, dark red, curve is the pulse results corresponding to the top DC curve (narrow blue trace).

Scope Shot

The scope-shot UTM is a general purpose utility that is used for validation, troubleshooting and for prototyping transient tests. This UTM applies a pulse train to the DUT gate and a DC bias to the DUT drain with a fixed set of values. The returned data is the scope waveform data, as shown in Figure 13.

The gate signal is the positive pulse curve (blue), using the left Y axis. This curve is the pulse applied to the DUT gate as measured at the scope card after the pulse has been split by the power splitter. The drain signal is the negative pulse (red), using the right Y axis. This negative curve is the response of the DUT drain. The applied drain voltage is DC, but the pulse applied to the gate causes the pulsed response of the drain. The drain response is a negative voltage due to the direction of the current flow through the sense resistor, in relation to the scope card measurement. See waveform E in Figure 1a and 1b.

Since scope-shot does not have auto-ranging capability, adjusting the values for GateRange and DrainRange will be necessary to get the best data. Note that this waveform data is raw and does not have any Pulse IV calibration factors applied, making it useful for a wide range of pulse tests and interconnect configurations.

To get approximate Pulse IV measurements for Vg:

1. Take an average of the points on the blue curve from time = 85 to time = 100 ns, giving 1.84V.
2. Multiply this average of Ch1out by 1.36 (typical cal factor for divider loss and cable losses), so the voltage seen by the gate in Figure 13 would be Vg ≈ 1.84 x 1.36 = 2.50 V.

To calculate the approximate drain current, Id:

1. Take an average of the points on the red curve from time = 90 to time = 105 ns, giving 315 mV.
2. Now convert the average voltage of Ch2out to current by dividing by the 50 Ω sense resistor: 315 / 50 = 6.3 mA.
3. Multiply this current by a representative cal factor of 1.02, giving Id ≈ 6.3 x 1.02 = 6.43 mA.

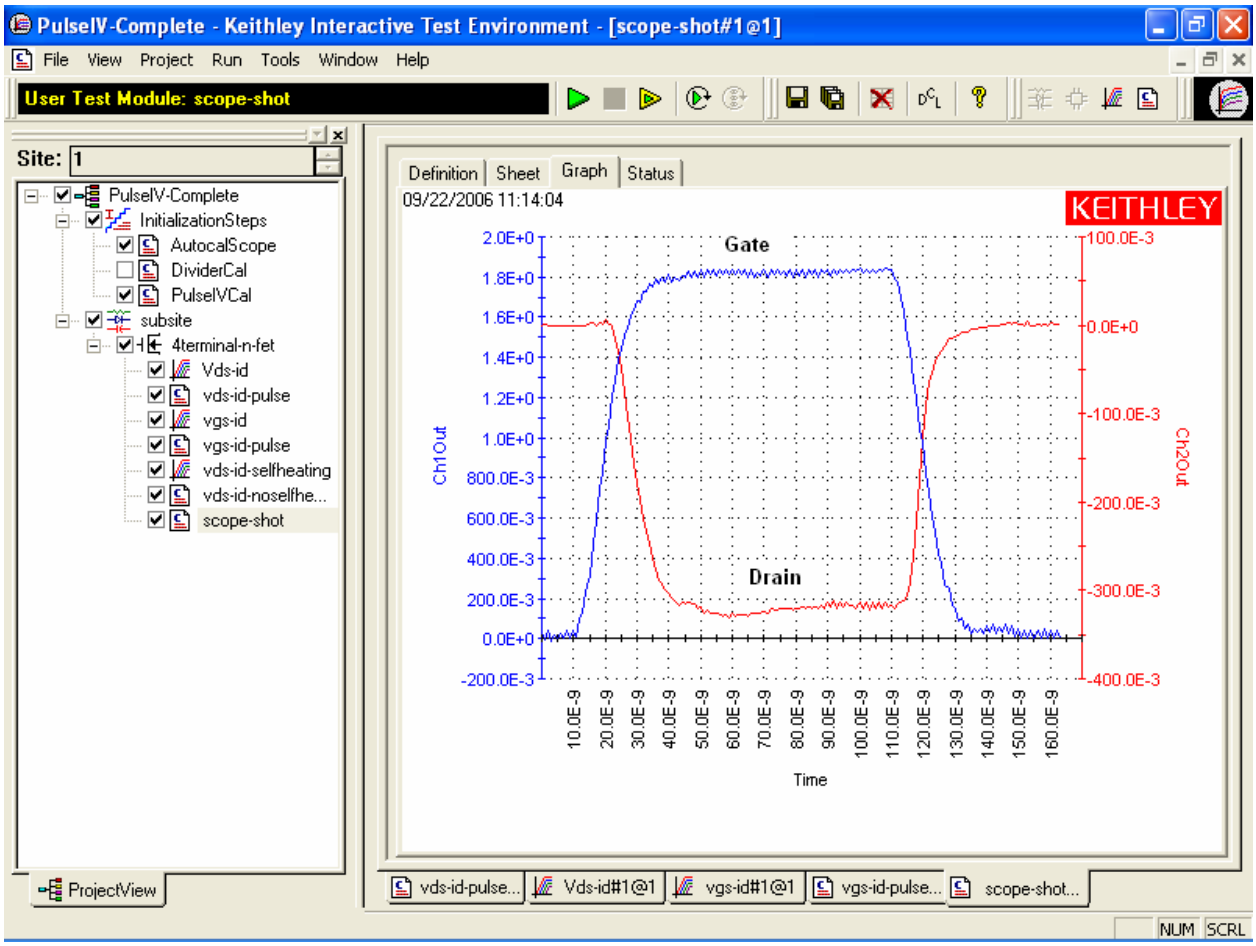

Figure 13. Scope-shot UTM graph tab, showing a result for a 100 ns wide pulse. The positive pulse curve (blue), using the left Y axis, is the gate voltage seen at Channel 1 of the 4200-SCP2. The negative pulse curve (red), using the right Y axis, is the Vd response voltage seen at Channel 2 of the 420-SCP2. These values are not calibrated. To get drain current, divide the Vd response curve by 50 ohms.

Prober Interconnect

The 4200-PIV package provides both DC and Pulse capability to the DUT pins without re-cabling or switching. The key to this capability is the 4200-RBT Remote Bias Tee, which uses passive electrical components to combine the low frequency DC signals with the high frequency pulse signals. For further information on the 4200-RBT, see section 11 in the 4200 Reference Manual.

The cabling from the 4200-RBT is SMA coax, which will connect to many RF and DC probe manipulators.

DC Prober Interconnect

For DC structures, an adapter cable (4200-PRB-C, Figure 14) is included to convert from the SMA to dual SSMC connections on DC manipulators.

Many DC probe manipulators are available with SSMC connections at the probe needle holder.

- Cascade DCM-2xx Kelvin DC probe manipulators
- Suss Microtec probe tips
- Signatone SCA-50 coaxial probes
- American Probe & Technologies
    - 74CJ series coaxial probe holder
- Any probe interconnect with SSMC connectors near the probe tip

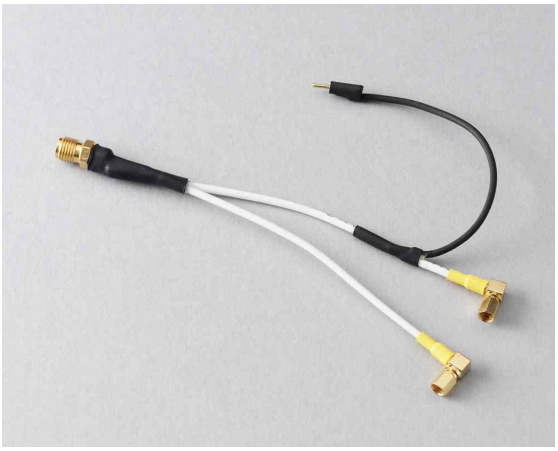

Figure 14. 4200-PRB-C 4200 Pulse SMA to SSMC Y Adapter

These SMA to SSMC Y adapter cables are appropriate for on-wafer pulse IV testing of nominally DC structures (Figure 15). These “Y” cables are not appropriate for higher frequency devices. The upper frequency limit is not specified, because the effect of actual device layout and probe configuration can have a significant impact. In general, any device that has an F_T much above 1 GHz might oscillate when using a DC probe connection scheme and the 4200-PRB-C cables.

For additional information see the documentation included with the 4200-PRB-C (PA-928).

RF Prober Interconnect

If the device has an RF layout (G-S-G), the Y adapter cables and DC probe manipulators will most likely be insufficient. In the case of RF G-S-G pad layout, do not use the 4200-PRB-C Y cables, just use the shorter SMA cables (6”/15 cm) supplied with the 4200-PIV package to connect directly from the 4200-RBTs to the RF manipulators (Figure 16). Note that the 4200-RBT with the power divider is connected to the Gate.

Setting up for Pulse IV

1. Set up the 4200-SCS, referring to the 4200-SCS Quick Start Guide and 4200-SCS Reference Manual.
2. Set up and connect the 4200-PIV. For 4200-PIV set up, refer to the 4200-SCS Applications Manual, along with Figure 2 and 3. Use the supplied torque wrench for the SMA connections on the 4200-RBTs, power divider and manipulators. Use care when installing the cable to the 4200-SCP2 trigger SMB connector.
3. For RF probes, connect the SMA cables from the 4200-RBTs to the RF probe manipulators, as shown in Figure 16. Skip Step 4 and go to Step 5.
4. For DC structures, prepare the probe connection by disconnecting all DC cables from the SSMC connectors on the needle holders. Continue setup of PIV by connecting a 4200-PRB-C cable to the 15 cm (6 inch) SMA cable attached to each 4200-RBT. Refer to Figure 15. Don't forget to connect the black shield jumpers to each other as shown in the middle of Figure 15. Connecting shields together is necessary and very important, as it greatly reduces the inductance that is caused by the loop area of the interconnect.
5. Finish setup by verifying connections and running a scope-shot test using the 4200 Project Pulse IV-Complete.

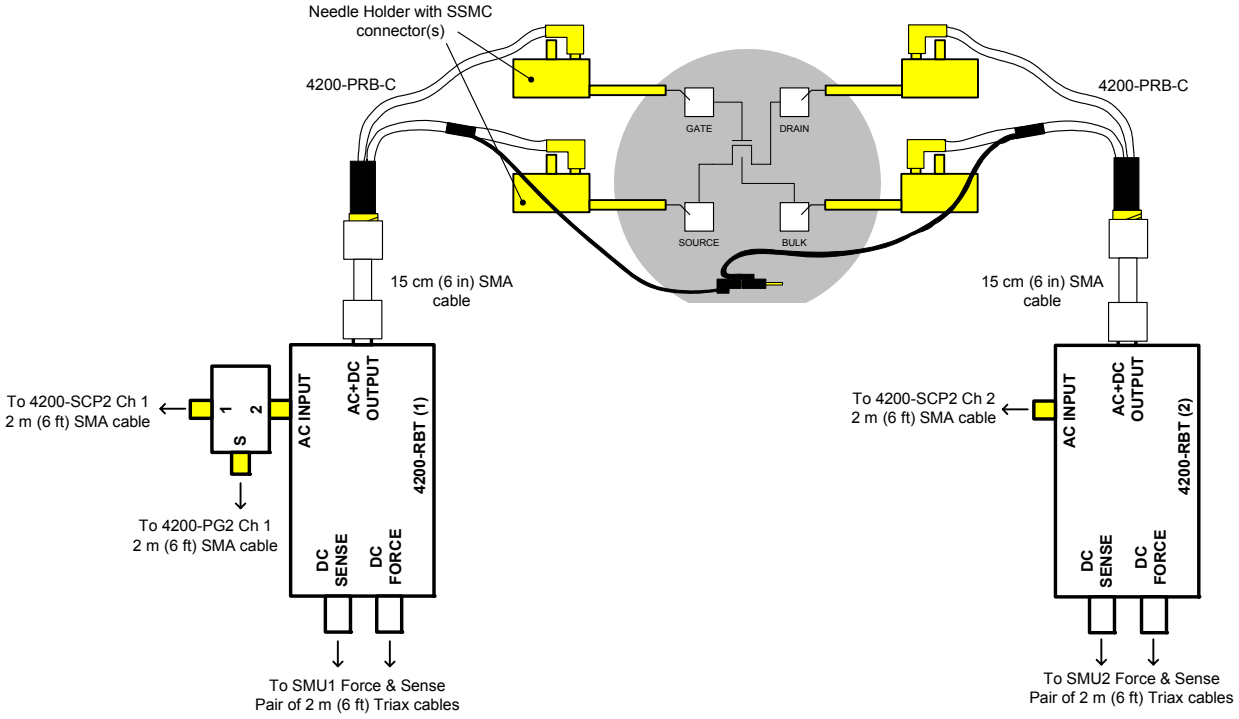

Figure 15: Pulse IV connections from Remote Bias Tees to DC probes for a DC layout DUT structure, using the 4200-PRB-C Y adapter cable.

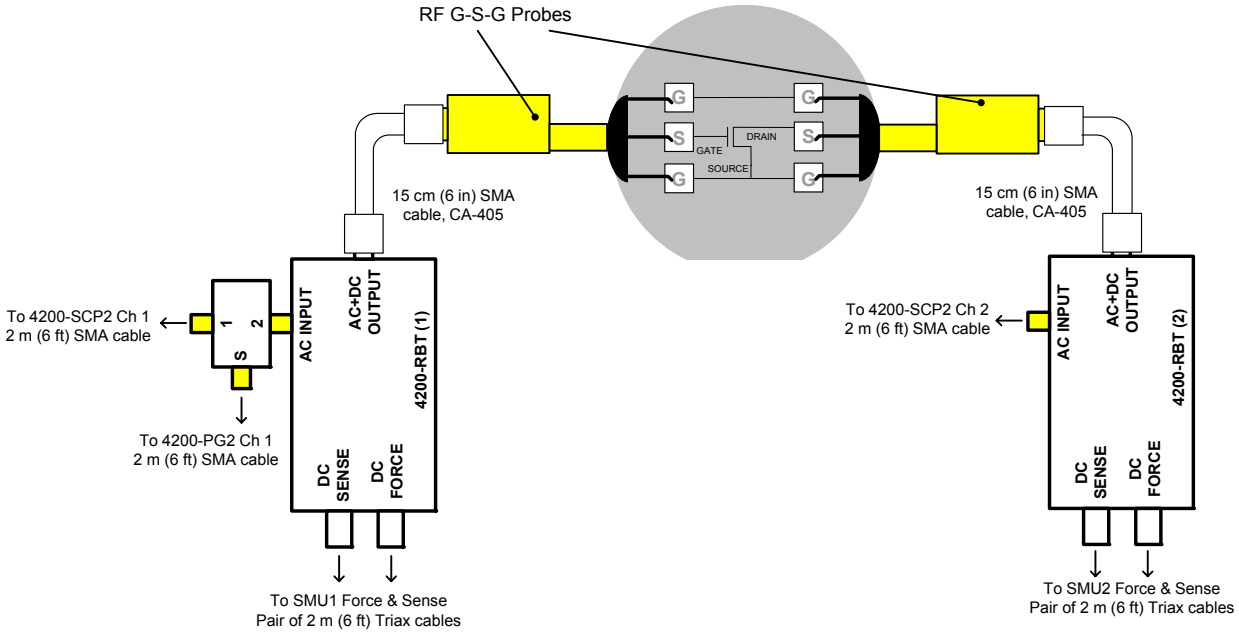

Figure 16. Pulse IV connections from Remote Bias Tees to RF G-S-G probes for RF.

Using 4200 Project PulseIV-Complete for the first time

NOTE: These instructions were written for the PulseIV tests available in KITE 6.1.

1. Connect up the 4200-PIV as documented above.
2. If KITE is not running, start KITE by double-clicking the KITE icon on the 4200 desktop.
3. Open the PulseIV-Complete project. Or, click FILE > Open Project > if necessary, move up one level at the Open Project file window to the display the Projects directory. Double-click PulseIV-Complete folder, then double-click Pulse IV-Complete.kpr to open the project.
4. The screen should resemble the screen shot in Figure 4. The right portion of the screen may not be the graph shown, but the project navigator should match that shown in Figure 4.
5. Connect or touch-down on the chosen device under test (DUT).
6. Verify setup.
    a. Step 1: Follow the instructions for “Running scope-shot” to validate proper setup and operation of the PIV package. Ensure that both the gate and drain waveforms are visible and do not have any significant ringing or overshoot (Figure 13).
    b. Step 2: Try running Vds-id-pulse (“Running Vds-id-pulse”) and/or Vgs-id-pulse (“Running Vgs-id-pulse”) and look for a characteristic response. If desired, DC IV tests may also be run (“Running Vds-Id”, “Running Vgs-id”). Once both the scope-shot and a pulse IV test have been verified, pulse system calibration can be performed.
7. Calibration: Follow “Running AutocalScope” and “Running PulseIVCal” in this document to perform the necessary pulse calibrations.
8. Use: After successful pulse calibrations, the system is now ready to be used for pulse and DC characterization of transistor devices.

Running AutocalScope

AutocalScope should be run before any pulse calibration is performed. For best Pulse IV results, the AutocalScope should also be run before the first experiments of the day.

1. The 4200-SCS should be turned on at least 30 minutes before performing any calibration or measurements.
2. Double-click AutocalScope in the Project Navigator (Figure 4).
3. Click the green Run button.
4. Follow the instructions given on the pop-up dialog box and disconnect all connections to the 4200-SCP2.
5. The SCP2 performs an autocal, which takes about 1 minute.
6. The test is complete when the Run button is green. In the Sheet tab, an AutoCalStatus=0 means that there were no errors.
7. Reconnect the cables to the 4200-SCP2. Use care when installing the cable to the 4200-SCP2 trigger SMB connector.

Running PulseIVCal

Verify proper setup by running a scope-shot. For on-wafer testing, have a through, or short, structure available, or ensure that sharing a pad for both the gate and drain probes provides a good connection. There are two steps to the calibration, open and through/short.

1. If not already performed, run the AutocalScope procedure above.
2. Double-click PulseIVCal on the Project Navigator.
3. Click the green Run button to start the PulseIVCal.
4. Click OK on the first dialog box to continue the PulseIVCal (Figure 17, left dialog box).
5. The second dialog box requests that the probe pins be raised from the wafer, breaking contact. Raise probe pins or lower wafer to create the Open condition.
6. Click OK on the Open dialog box (Figure 17, middle dialog box). The Open portion should take about 1 minute.
7. The third dialog box requests that the probe pins be connected to each other via a through device. Lower the probes onto a through device.
8. Click OK on the Through dialog box (Figure 17, right dialog box). The Through portion should take about 1 minute.
9. The test is complete when the Run button is green. In the Sheet tab, a cal_pulseiv=0 implies that there were no errors.
10. The system is now ready to test regular devices.

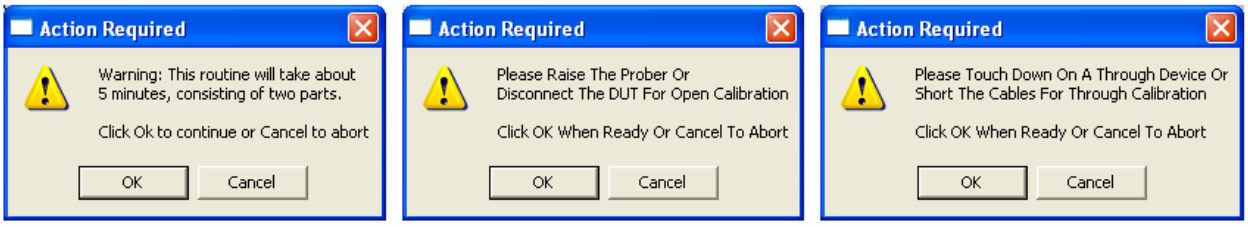

Figure 17. Three separate PulseIVCal dialog boxes: Initial, Open Cal, Through Cal.

Running Vds-id DC ITM

The default settings sweep the drain from 0-4V in 100 mV steps while stepping through three gate voltages: 1.5, 2.0, 2.5V (Figure 5, 6). When changing these settings, note the voltages and step size used so the same settings can be used in Vds-id-pulse.

1. Double-click Vds-id ITM in the Project Navigator.
2. Click the green Run button. Three 3 Vds-id curves will be measured and displayed on the graph.

Running Vds-id-pulse UTM

The default Vds-id uses the same drain voltage settings as the DC Vds-id. The Vds-id-pulse (Figure 4, 7) does not have the automatic step capability of the DC Vds-id. To run the 3 gate voltages, perform the following.

1. Ensure that the VdStart, VdStop, VdStep match the values in the DC Vds-id. To sweep from a high to a low voltage, enter voltages so that VdStop < VdStart and use a negative value for VdStep. If any values need to be modified, remember to press the Enter key after typing in the value.
2. Set Vgs to the first voltage. The default is 1.5V. Make sure to press the Enter key after typing in the value.
3. Click the green Run button.
4. After the test is finished, set Vgs to the second voltage. The default is 2.0V.
5. Click the yellow and green Append button.
6. After the test is finished, set Vgs to the third voltage. The default is 2.5V.
7. Click the yellow and green Append button.
8. To add or update DC results on the pulse Graph, follow the instructions, “Comparing DC and Pulse Results.”

Running Vgs-id DC ITM

The default settings sweep the pulses on the gate from 0-2V in 50 mV steps and set the drain voltage to 1 V (Figure 8, 9). When changing these settings, note the voltages and step size used so the same settings can be used in Vgs-id-pulse.

1. Double-click Vgs-id ITM in the Project Navigator.
2. Click the green Run button. The Vgs-id curve will be measured and displayed on the graph.

Running Vgs-id-pulse UTM

The default Vgs-id (Figure 10, 11) uses the same default settings as the DC Vgs-id.

1. Ensure that the Vds, VgStart, VgStop, VgStep match the values in the DC Vgs-id. To sweep from a high to a low voltage, enter voltages so that VgStop < VgStart and use a negative value for VgStep. If any values need to be modified, remember to press the Enter key after typing in the value.
2. Click the green Run button.
3. To add or update DC results on the pulse Graph, follow the instructions, “Comparing DC and Pulse Results.”
4. To reduce noise, the smaller subthreshold currents of this test require a larger number of measurements to be averaged. Use Average = 20-25 for best results. Averaging a larger number of pulses provides a decreasing advantage.

Running scope-shot

Scope shot (Figure 13) is used to verify proper connection and system setup. The waveform shown in figure 13 is a typical result; actual results should be similar. If waveform has significant ringing or overshoot, the pulse IV tests will not provide good results. Check the pulse interconnects to ensure proper cablings and ensure all connections are tight. If using 4200-PRB-C (Y adapter cable for pulsing with DC interconnect and structures), ensure that the two ground lugs are connected together.

The positive pulse curve (blue) is the pulse applied to the gate, as seen at the scope. Note that the displayed waveform data does not have any calibration factors applied. This means that the sourced pulse to the gate is lower than expected when used in the default pulse IV setup. To get approximately correct gate pulse voltage, multiply the waveform data by 1.36 to get the voltage applied to the DUT gate pin. The negative pulse curve (red) is the drain response.
The scope-shot UTM has more parameters than the other Pulse IV routines, such as rise/fall times and DC offsets, so it can also be used for investigating or prototyping single pulse transient tests.

Adjustable parameters:

PulseWidth	Vgs pulse width, full width half maximum (FWHM)
PulseAmplitude	Vgs, gate voltage pulse
GateRange	SCP2 gate voltage range, manual setting, the SCP2 range is centered around zero, so the 5V range on the scope covers -2.5V to +2.5V. As an example, for a 3V signal, use GateRange = 10 (-5V to +5V), not 5 (-2.5 to +2.5V). Available ranges for the 4200-SCP2: 0.05, 0.10, 0.25, 0.5, 1, 2, 5, 10 V.
DrainRange	SCP2 drain voltage range, manual setting. To calculate the appropriate range, use DrainRange = (Estimated Id) x 50 x 2. See above for valid SCP2 ranges.
PulsePeriod	Vgs pulse period. When using the Pulse IV setup with 4200-RBTs, use a PulsePeriod ≥ 1000 x PulseWidth, to keep the pulse duty cycle ≤ 0.1%. For most cases, it is best to use 200E-6, which will allow an appropriate duty cycle across the range of supported 40-150 ns pulse widths.
AverageNum	Number of pulses to average. For larger currents, Id ≥ 500 uA, AverageNum = 5 is usually sufficient. For smaller Id, use 20-25. Larger values provide minimal additional improvement. Note that all pulse IV tests have this setting, which controls how many pulses are used to return a result, not how many pulses are sent to the DUT.
DrainBias	Vd, DC voltage on DUT drain
VPUID	4200-SCP2 identification string. VPUID = VPU1.
DrainSMU	SMU for Vd. Default is SMU2, but any other available SMU may be used.

All other parameters may be used for single pulse studies or other investigation. For example, the rise and fall time can be varied in scope-shot, which is useful for transient, single pulse, tests. This routine has minimal parameter checking to permit the widest possible range of values.

Comparing DC and Pulse Results

Using the easily accessible data in the Sheet tab of KITE, it is simple to compare results between tests. This procedure explains how to copy the DC results into a pulse UTM to allow comparison between pulse and DC IV results in a single graph.

1. Double-click Vds-id ITM in the project navigator.
2. Click the Sheet tab.
3. Choose the desired results worksheet. If there is only one set of curves, then the results are in the Data tab. If additional tests have been appended, choose the desired Append tab.
4. Highlight all of the data in the desired worksheet by clicking the upper-left “cell” as shown in Figure 18.

5. Copy the data by right-clicking and choosing Copy, as shown in Figure 19, or use Ctrl-C.
6. Double-click on Vds-id-pulse UTM.
7. Click the Sheet tab.
8. Click the Calc worksheet tab.
9. Click the upper-left cell, A1.
10. Paste DC data into pulse Calc worksheet by right-clicking and choosing Paste, as shown in Figure 20, or use Ctrl-V. If there is previous data in the Calc worksheet, it is not necessary to delete it. Now all comparison DC and pulse data is located in the same test, but we need to define the graph to display the DC data located in the Calc worksheet.
11. Click on the Graph tab.
12. Right-click on the graph and choose the first option, Define Graph.
13. In Figure 21, click the middle column, Y1, to add the appropriate DC curves. In this case, 3 Vds-id curves have been added: DrainI(1), DrainI(2), DrainI(3). Note that all 3 of these Data Series are located in the Calc worksheet, as noted in the Sheet column in Figure 21.
14. Now all 3 curves are added to the pulse graph, as shown in Figure 4. To change graph colors or add data point shapes, move the cursor along the desired curve until the pointer appears. With the pointer displayed, right-click to get the Data Series Properties dialog box. The Shape property determines how each data point is demarcated.
15. To verify pulse operation, use a DUT that does not exhibit any self-heating or transient charging effect. In a properly configured and calibrated system, the pulse IV results should correlate to the DC results within ±4%, with many results ≤ 2%, when testing a device that does not exhibit heating or charging effects.

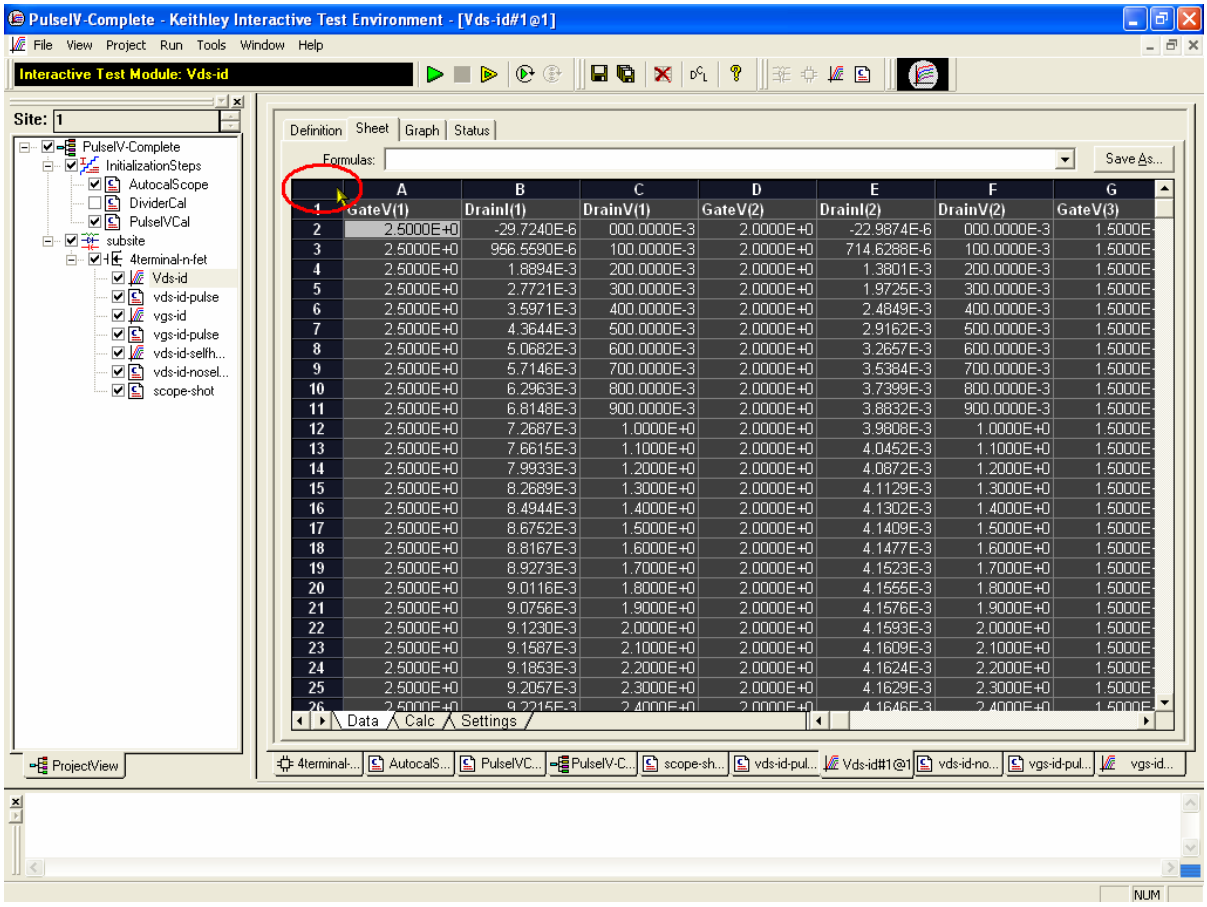

Figure 18. Highlighting all entries in a worksheet. Screenshot shows all data highlighted after clicking circled area.

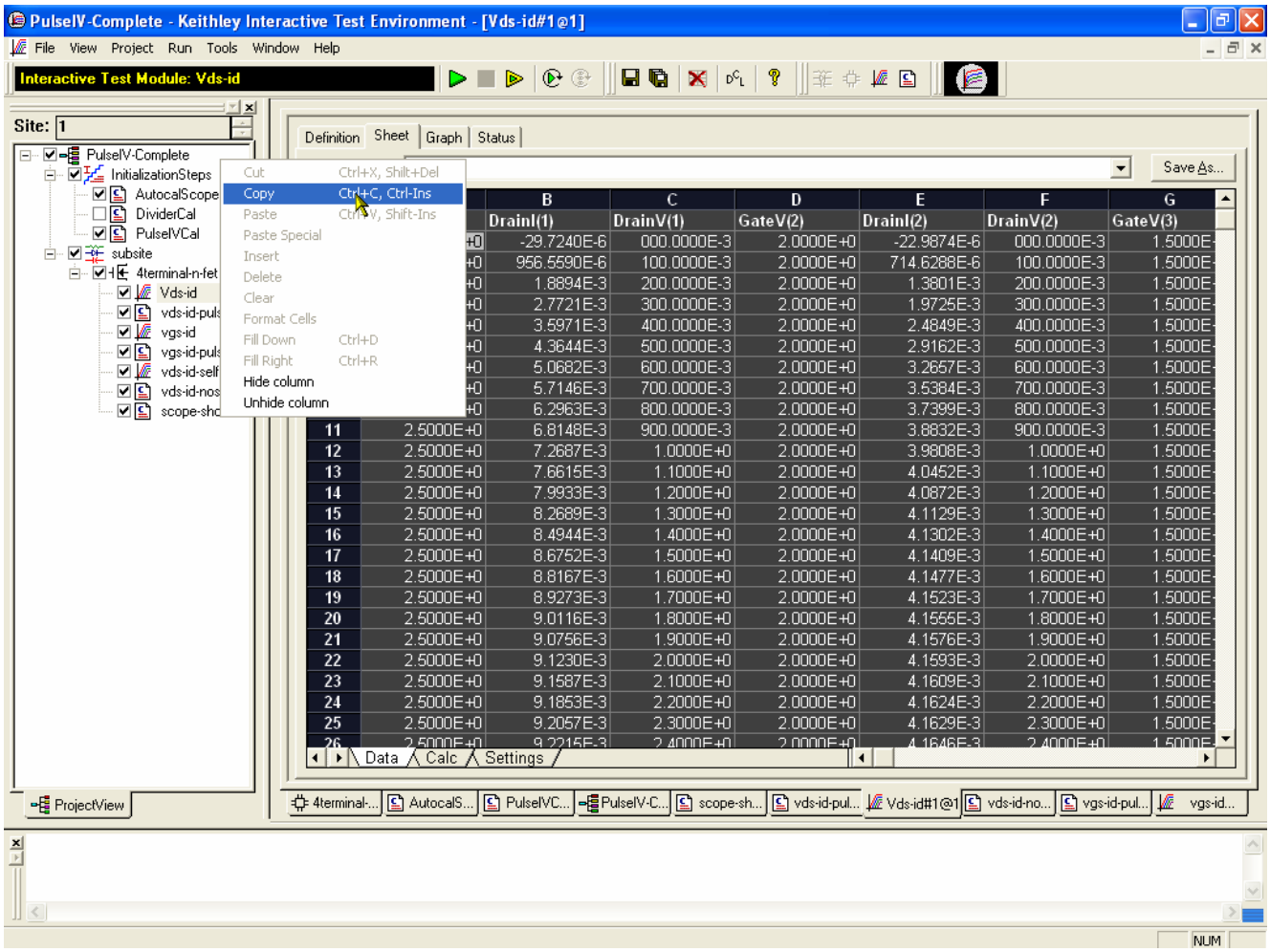

Figure 19. Copy data by right-clicking worksheet and select Copy.

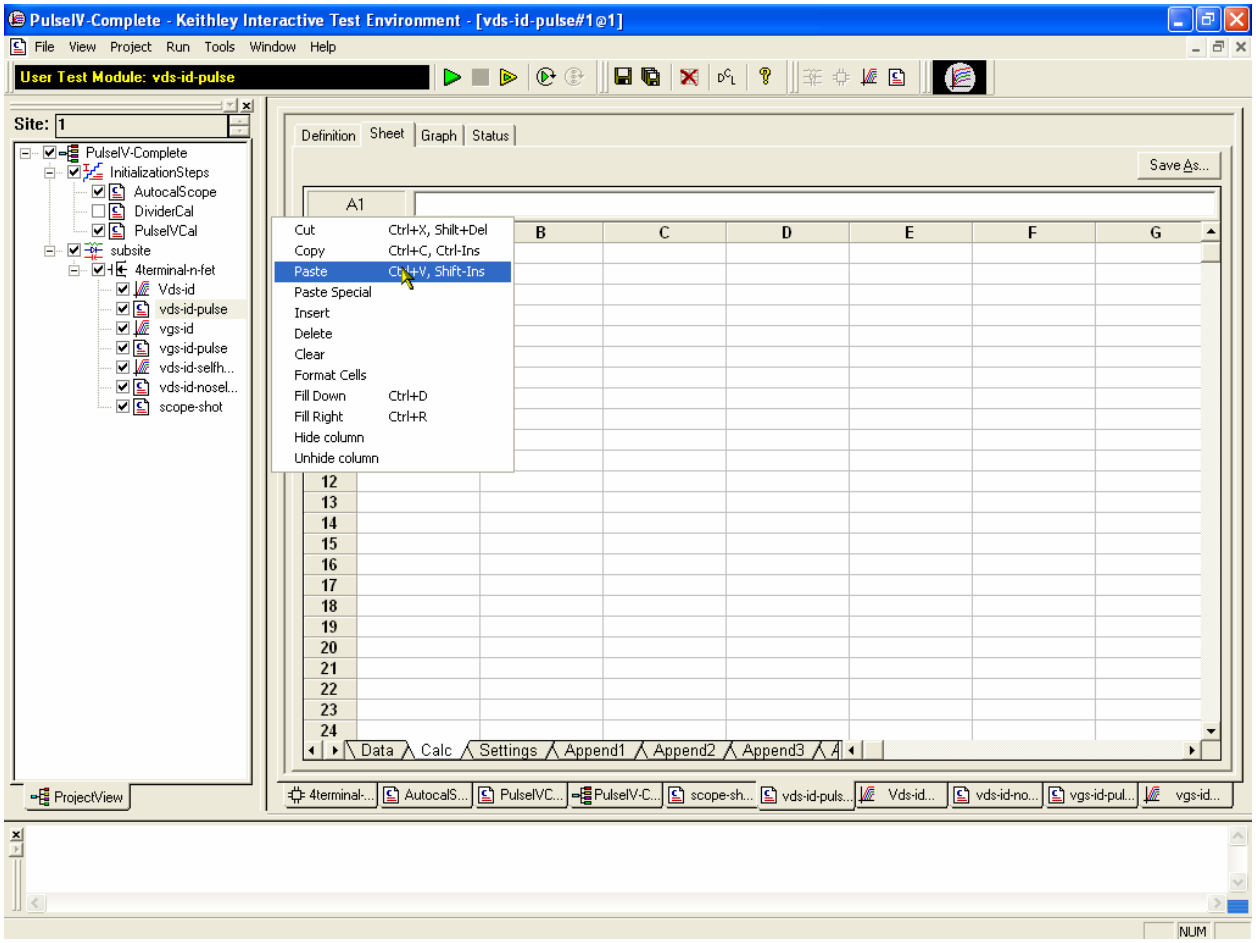

Figure 20. Paste data into pulse test Calc worksheet.

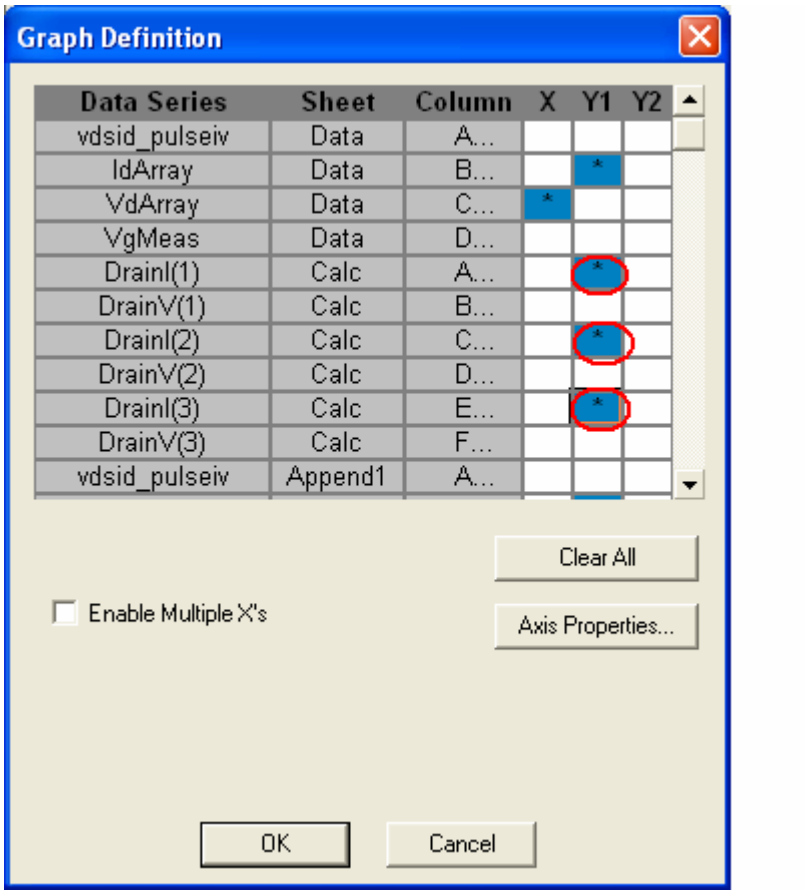

Figure 21. Define graph dialog box with the 3 added DC curves circled.

Tips for using Pulse IV

- Confirm connection: Use scope-shot as the first test after touching down on a device to confirm that there is proper connection to the DUT, *before* running any pulse test.
- Always calibrate after any setup changes (new probe tips or manipulators, cable replacement)
- Proper pulse IV performance can be verified by testing a device that does not exhibit any self-heating or charge trapping effects and comparing DC to pulse results.
- Use Ave = 5 for higher drain currents (> 500 uA). Use Average = 25 (or higher) for Id < 500 uA.
- Pulse IV measurements have less resolution and sensitivity than typical DC results, so test parameters, such as averaging or smaller steps sizes, and post-test processing, such as curve fitting, may be required to obtain roughly equivalent results.

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2. A. Kerber, E. Cartier, L. Pantisano, M. Rosmeulen, R. Degraeve, T. Kauerauf, G. Groeseneken, H. E. Maes, and U. Schwalke, "Characterization of the VT instability in SiO2/HfO2 gate dielectrics," Proc. IEEE., IRPS pp. 41, 2003.

3. C. D. Young, R. Choi, J. H. Sim, B. H. Lee, P. Zeitzoff, Y. Zhao, K. Matthews, G. A. Brown, and G. Bersuker, “Interfacial Layer Dependence of HfSixOy Gate Stacks on Vt Instability and Charge Trapping Using Ultra-short Pulse I-V Characterization,” Proc. IEEE IRPS, p. 75-79, 2005