

Testing Flash Memory with the Model 4200-SCS



Flash Memory

Floating gate non-volatile memory: programmed and erased by charge tunneling or hot electron injection

Two main technologies

- Nor
- Nand

Two main sets of tests for each technology

- Characterization
- Lifetime

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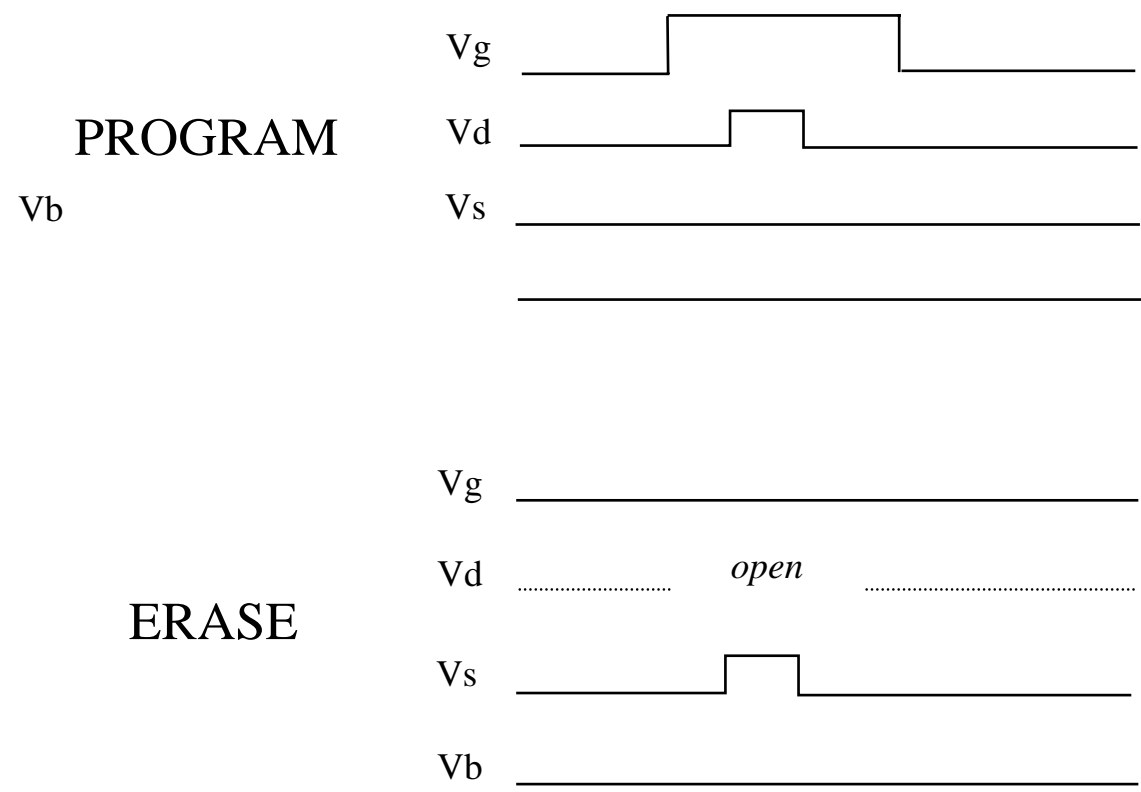
NOR vs. NAND

Parameter	NAND	NOR
Nonvolatile	yes	yes
Random Access	No	yes
Write Cycles	10^6	10^6
Read Time	$25\mu\text{S}$	70nS
Write Time/Voltage	$300\mu\text{S}$ < 20V	$1-10\mu\text{S}$ < 13V
Erase Time/Voltage	$900\mu\text{S} - 5\text{mS}$ < 20 V	$10-100\text{mS}$ -13 to -10V

*Source: *Prospect of Emerging Nonvolatile Memories*, Hongsik Jeong & Kinam Kim, Materials Research Society Symposium Proceedings, Vol. 830, p 366

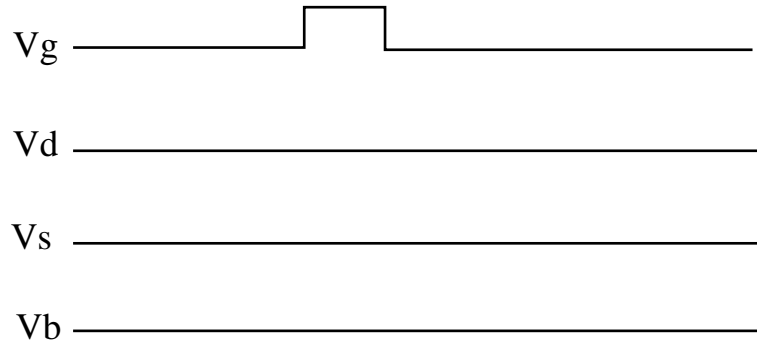


Typical NOR program/erase cycle

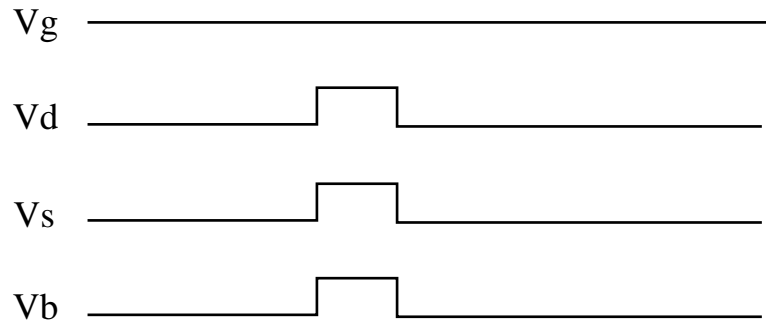


Typical NAND program/erase cycle

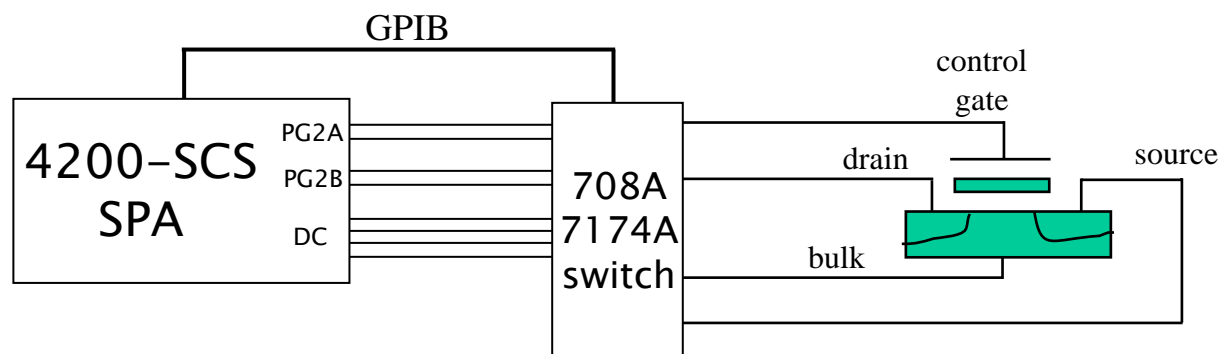
PROGRAM



ERASE



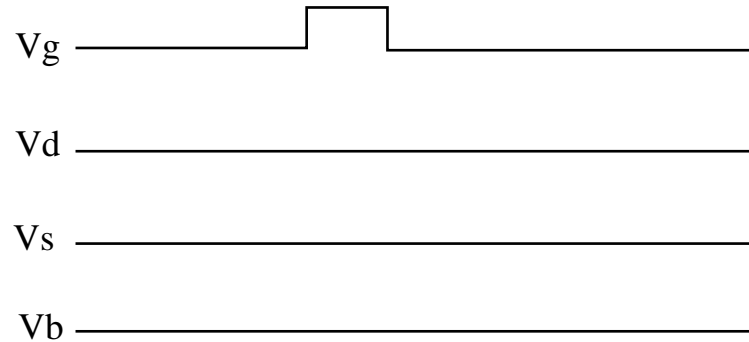
Proposed NAND Flash test setup



- Allows easy switching between Pulse and DC tests
- PG2 channels can be used as DC bias during program/erase – minimizing switching
- Pattern generation/multi-segment pulse capabilities of PG2 allow for program/erase cycle to be setup as one pattern and repeated n times for lifetime testing

NAND program/erase cycle performance

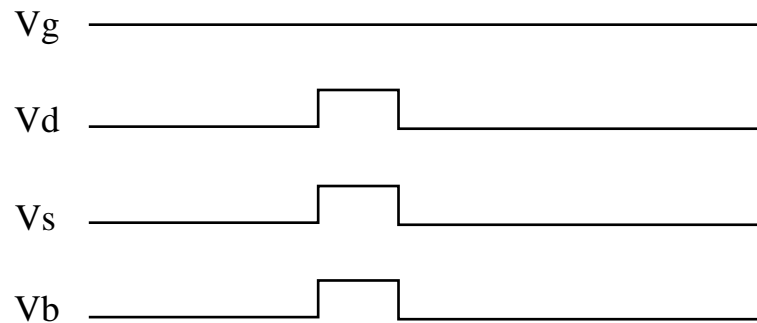
PROGRAM



Vg pulse capabilities

- $\pm 10V$
- min rise/fall = 100ns
- min pulse width = 100ns

ERASE

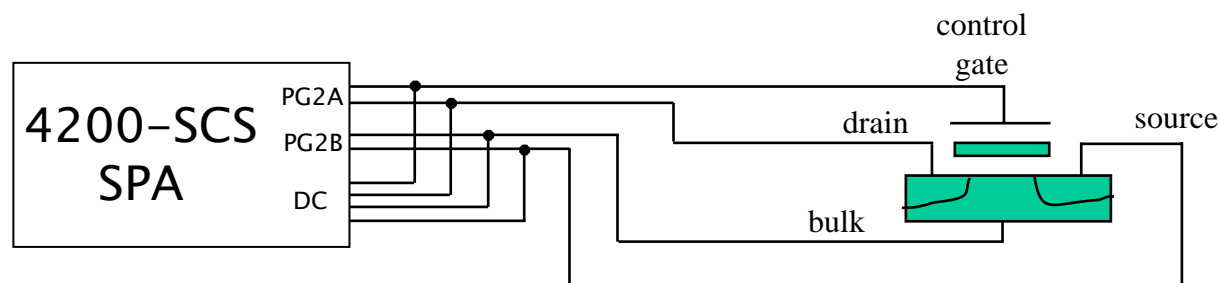


Vd, Vs, Vb pulse capabilities

- $\pm 20V$
- min rise/fall = 100ns
- min pulse width = 250ns



Alternate NAND Flash test setup



- Pulse and DC have output relays – open DC relays when Pulsing, open Pulse output relays when DC testing
- PG2 channels can be used as DC bias during program/erase
- Easy connect, less flexibility
- Pattern generation/multi-segment pulse capabilities of PG2 allow for program/erase cycle to be setup as one pattern and repeated n times for lifetime testing

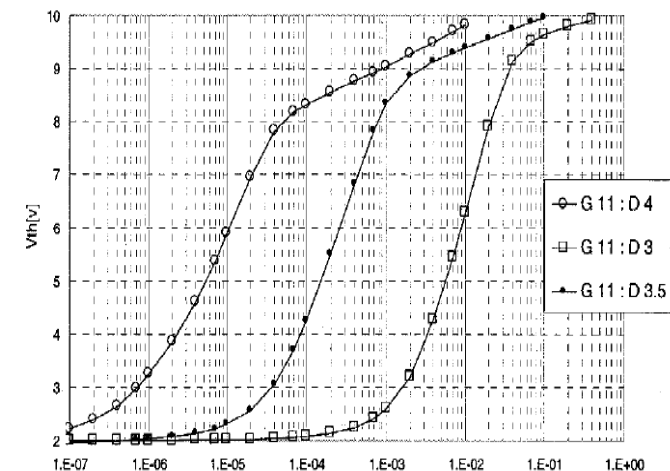
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NAND Flash performance testing

Sample tests:

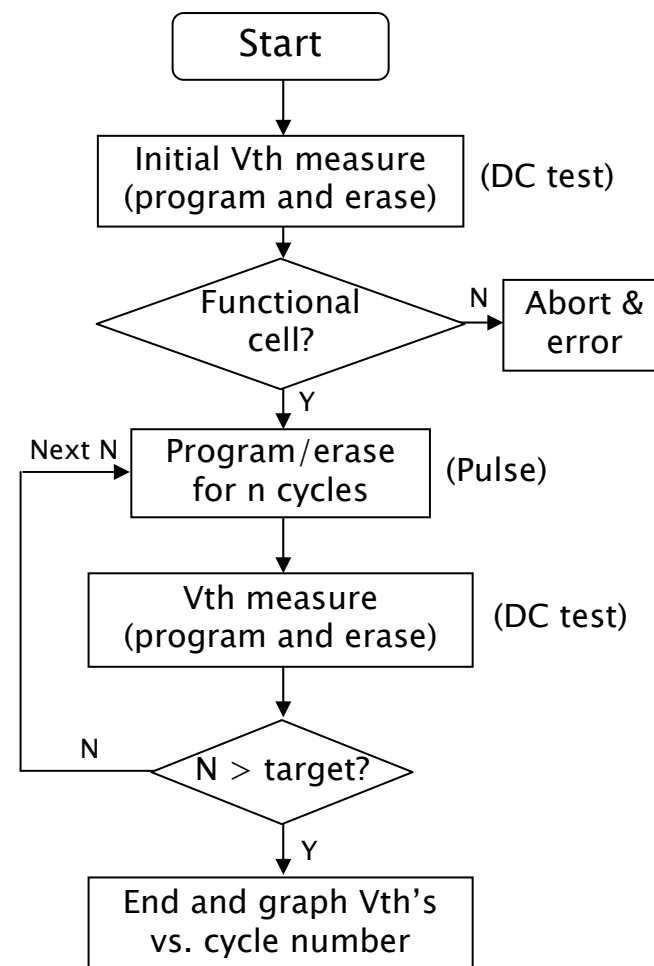
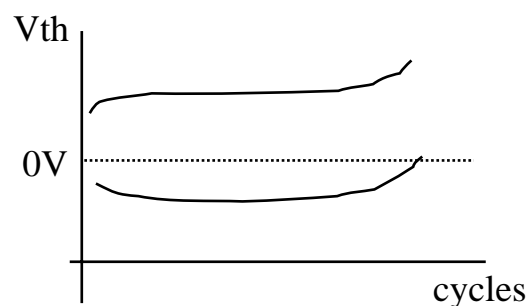
- Program characterization
 - Sweep program width, measure V_{th} between each program cycle, graph V_{th} vs. Program PW
 - Sweep program voltage, measure V_{th} between each program cycle, graph V_{th} vs. Program voltage
- Erase Characterization: similar to Program tests
- Disturb Test
 - Tbd for NAND

V_{th} vs. Program pulse width



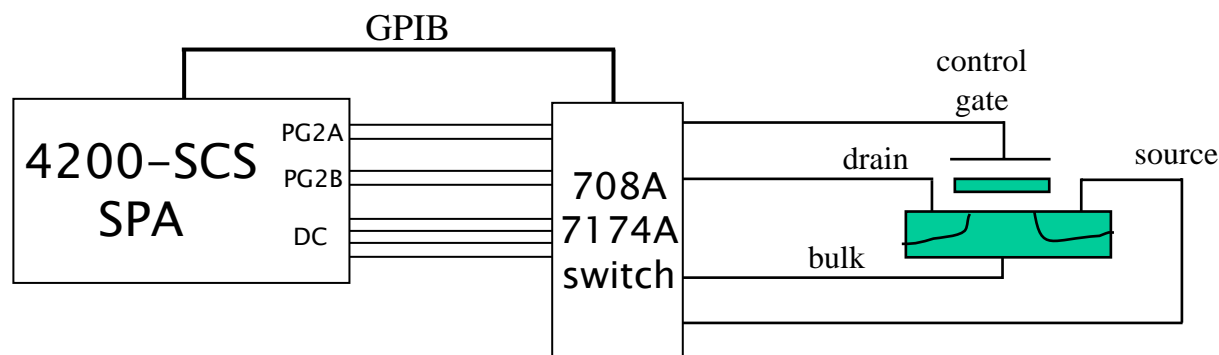
NAND Flash endurance testing

- Stress-Measure
- Stress: series of program/erase cycles
 - Each program/erase cycle is the same
 - User control of cycle specifics (pulse widths, voltages, pulse delays and synchronization)
- Measure: test V_{th} at specific cycle points
 - User controllable: i.e. 3 measures per decade
- Graph V_{th} vs cycle number (log scale)



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Proposed NOR Flash test setup

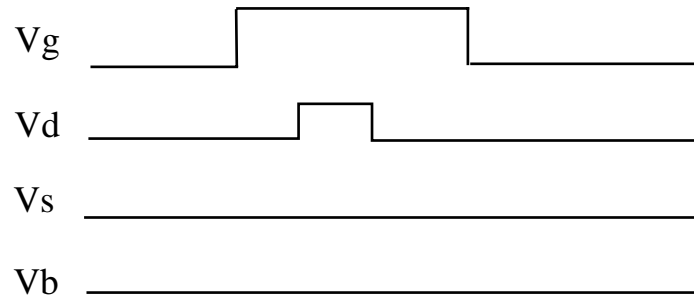


- Allows easy switching between Pulse and DC tests
- Solid-state relay on output of PG2 for lifetime testing (open drain on erase)
- PG2 channels can be used as DC bias during program/erase – minimizing switching
- Pattern generation/multi-segment pulse capabilities of PG2 allow for program/erase cycle to be setup as one pattern and repeated n times for lifetime testing (segment can control solid-state output relay)

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Typical NOR program/erase cycle

PROGRAM



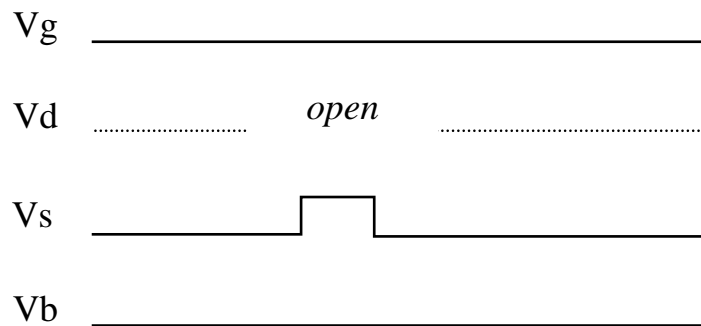
Vg pulse capabilities

- $\pm 10V$
- min rise/fall = 100ns
- min pulse width = 100ns

Vd pulse capabilities

- $\pm 20V$
- min rise/fall = 100ns
- min pulse width = 250ns

ERASE

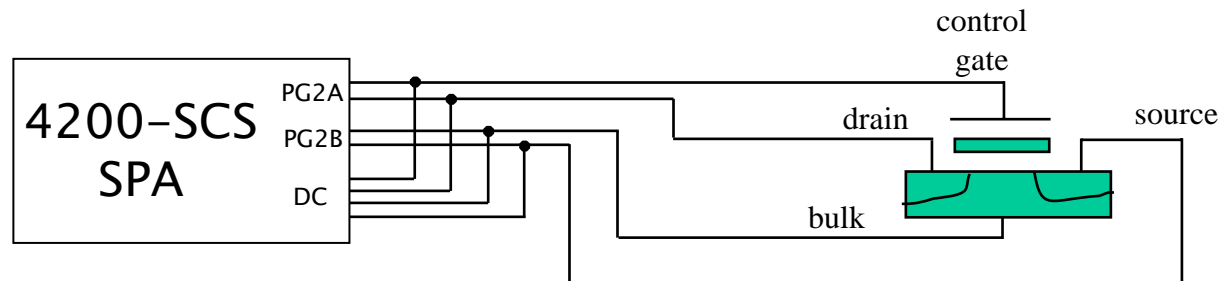


Vs pulse capabilities

- $\pm 20V$
- min rise/fall = 100ns
- min pulse width = 250ns



Alternate Proposed NOR Flash test setup

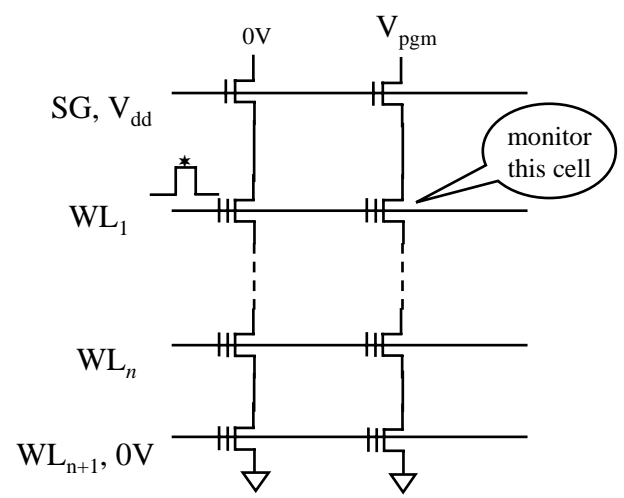


- Pulse and DC have output relays – open DC relays when Pulsing, open Pulse output (mechanical) relays when DC testing
- Solid-state relay on output of PG2 for lifetime testing (open drain on erase)
- PG2 channels can be used as DC bias during program/erase
- Easy connect, less flexibility
- Pattern generation/multi-segment pulse capabilities of PG2 allow for program/erase cycle to be setup as one pattern and repeated n times for lifetime testing

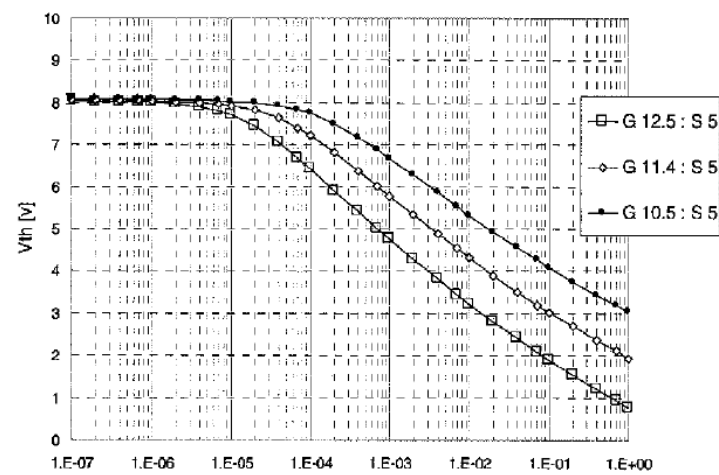
NOR Flash performance testing

Sample tests:

- Program characterization
 - Sweep program width, measure Vth between each program cycle, graph Vth vs. Program PW
 - Sweep program voltage, measure Vth between each program cycle, graph Vth vs. Program voltage
- Erase Characterization: similar to Program tests
- Disturb Test

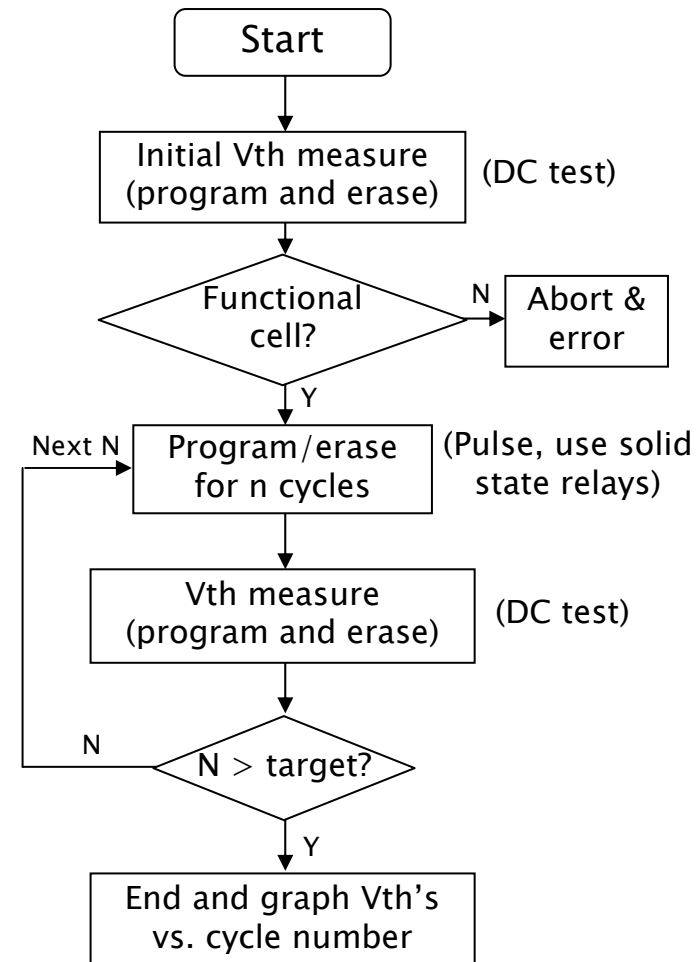
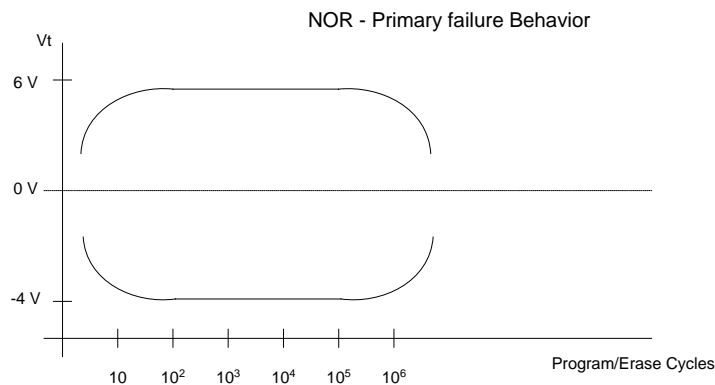


Vth vs. Erase Pulse Width



NOR Flash endurance testing

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END

